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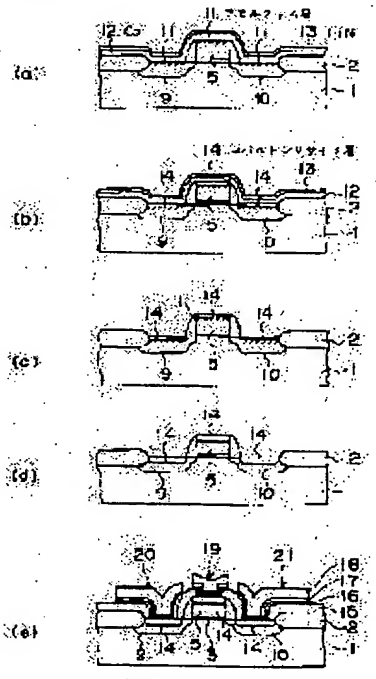
(54) MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To form a cobalt silicide layer wherein a spike is hard to occur on the bottom surface, relating to a manufacturing method for a semiconductor device containing a salicide process.
SOLUTION: On the upper layer part of an impurity diffusion layer 9 of a silicon, an amorphous layer 11 is formed by ion implantation, and after an cobalt film 12 is formed on the impurity diffusion layer 9, the cobalt film 12 and the silicon in the impurity diffusion layer 9 are made to react each other in the first thermal treatment, so that a cobalt silicide layer 14 made of CoSi or Co2Si at low temperature is formed on the upper layer part of the amorphous layer 11. Then, no-reaction cobalt is removed, and in the second thermal treatment, the CoSi or Co2Si constituting the cobalt silicide layer 14 is decomposed into CoSi2 for lower resistance, and at the same time, the cobalt silicide layer 14 is made protruded up to the depth of the initial amorphous layer 11 or further.



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CLAIMS

[Claim(s)]
[Claim 1] The process which introduces an impurity into the management of a silicon layer and forms an impurity diffused layer by heat treatment, The process which forms an amorphous layer in the management of said impurity diffused layer by carrying out the ion implantation of the element, The process which forms the cobalt film on said amorphous layer, and said cobalt film and said impurity diffused layer are heated with the 1st temperature. It is Co2Si to the management of said amorphous layer. Or the process which forms the cobalt silicide layer which consists of CoSi, The silicon in said impurity diffused layer, the process which removes said cobalt film which did not react, and by heating said cobalt silicide layer and said impurity diffused layer with the 2nd temperature said Co2Si or CoSi -- CoSi2 The manufacture approach of the semiconductor device characterized by having the process which forms said cobalt silicide layer more deeply than the same depth as said amorphous layer, or said amorphous layer while making it change.
[Claim 2] Said 1st temperature is the manufacture approach of the semiconductor device according to claim 1 characterized by being 450 degrees C or less.
[Claim 3] Said 2nd temperature is the manufacture approach of the semiconductor device according to claim 1 characterized by being lower than the temperature in the case of said heat treatment which is 500 degrees C or more and forms an impurity diffused layer.
[Claim 4] Said cobalt film is the manufacture approach of the semiconductor device according to claim 1 characterized by forming in the thickness of 8-20nm.
[Claim 5] The manufacture approach of the semiconductor device according to claim 1 characterized by forming a cap layer on said cobalt film before performing said heat treatment after forming said cobalt film.
[Claim 6] Said element is the manufacture approach of the semiconductor device according to claim 1 characterized by being germanium, silicon, and arsenic.
[Claim 7] Said germanium is 8x1013 atoms/cm2. An ion implantation is carried out above, the ion implantation of said silicon is carried out by two or more 8x1014 atoms/cm, and said arsenic is 8x1013 atoms/cm2 - 5x1014 atoms/cm2. The manufacture approach of the semiconductor device according to claim 6 characterized by carrying out an ion implantation.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a semiconductor device of having a salicide process, in more detail about the manufacture approach of a semiconductor device.
[0002]
[Description of the Prior Art] High integration of today's semiconductor device and speed-izing of high-speed-izing can be remarkable, and can enjoy now easily a high-speed three-dimension image processing, a high-speed communication link, etc. with a domestic personal computer and a domestic game machine. Such high performance-ization has been realized by only making size of a CMOS device detailed. The present CMOS device is in the mass-production phase of magnitude where gate length is about 0.35 micrometers, and the 0.1 -0.05micrometer CMOS device is also reported by research level. However, the parasitism resistance according to a scaling law becomes large, and the engine performance does not go up as the conventional trend by the device with which gate length becomes smaller than 0.35 micrometers. Then, the process which silicide-izes the gate, the source, and a drain to coincidence, and forms them into low resistance to it, i.e., a salicide process, is an indispensable technique.
[0003] In the MOS transistor, if a diffusion layer is made shallow in order to suppress the short channel effect etc., since increase of resistance of a diffusion layer will be brought about, the technique which silicide-izes the polish recon front face which constitutes a gate electrode, and the front face of a source layer and a drain layer in self align, and forms them into low resistance is examined. As the silicide, ingredients, such as TiSi2, CoSi2, and NiSi, are used.
[0004] Next, the general production process of the MOS transistor which used Co Salicide for the surface of the gate, the source, and a drain is explained. First, drawing 20 (a) It is the silicon machine hill 101 so that it may be shown. It is LOCOS inside. Oxide film 102 It is about 50A gate oxide 103 by thermal oxidation about the front face of the separated field. It forms. Then, it is the polish recon film 104 of about 1500A thickness by the CVD method on it. It forms.
[0005] Next, drawing 20 (b) It is the polish recon film 104 so that it may be shown. After carrying out the ion implantation of either PORON, Lynn or arsenic inside, it is the polish recon film 104. Patterning is carried out and it is the gate electrode 105. It forms. The ion implantation of the next door is carried out next, and it is the shallow impurity impregnation layer 106. It forms. next, drawing 20 (c) it is shown -- as -- a CVD method -- silicon oxide with a thickness of about 1000A -- forming -- gate electrode 105 until it exposes -- anisotropic etching -- carrying out -- silicon oxide -- sidewall 107 ****** -- it leaves.
[0006] After that, the ion implantation of the next door is carried out, and it is the deep impurity impregnation layer 108. Impurity impregnation layer 106 shallow after forming Deep impurity impregnation layer 108 It is activated by heat-treatment and, thereby, is the gate electrode 105. Silicon substrate 101 of both sides Source layer 109 of LDD structure Drain layer 110 It will form. next, buffered fluoric acid -- the gate electrode 105, the source layer 109, and drain layer 110 after removing the silicon oxide (natural oxidation film) of each front face -- drawing 20 (d) it is shown -- as -- About 100A cobalt film 111 About 300A titanium nitride film 112 forming --

RTA for 550 ** 30 seconds (rapid thermal annealling) processing -- silicide ---izing -- cobalt silicide layer 113 It forms.
[0007] Then, drawing 20 (e) It is the titanium nitride film 112 so that it may be shown. The unreacted cobalt film 111 is removed and it is RTA for further 850 **30 seconds. It processes and, thereby, they are the gate electrode 105 and the source layer 109. And drain layer 110 The cobalt silicide layer 114 formed in the front face is further formed into low resistance. Such a Salicide technique is a fundamental process, as the amelioration technique, the flattening technique of a silicide layer is shown in JP,62-33466,A, and the equalization technique of the thickness of a silicide layer is indicated by JP,5-291180,A.
[0008]
[Problem(s) to be Solved by the Invention] When formation of the above cobalt silicide layers has a source layer and a deep drain layer, there is especially no problem, but when it becomes shallow, for example to about 100nm, there is a problem that leakage current becomes easy to flow. It thinks for the spike of cobalt silicide occurring from the bottom of a cobalt silicide layer, and running through a source layer and a drain layer as the cause. The spike of such cobalt silicide was produced even if formed according to the approach and temperature conditions which were indicated by two patent official reports which described the cobalt silicide layer above.
[0009] This invention is made in view of such a problem, and aims at offering the manufacture approach of a semiconductor device including the process which forms the cobalt silicide layer which a spike cannot produce easily on a base.
[0010]
[Means for Solving the Problem]
The process which introduces an impurity into the management of the silicon layer 1, and forms impurity diffused layers 9 and 10 by heat treatment so that the above-mentioned technical problem may be illustrated to drawing 1 and 2, (Means) The process which forms the amorphous layer 11 in the management of said impurity diffused layers 9 and 10 by carrying out the ion implantation of the element, The process which forms the cobalt film 12 on said amorphous layer 11, and said cobalt film 12 and said impurity diffused layers 9 and 10 are heated with the 1st temperature. The process which forms in the management of said amorphous layer 11 the cobalt silicide layer 14 which consists of Co2 Si or CoSi, Said impurity diffused layer 9, the silicon in ten and the process which removes said cobalt film 12 which did not react, and by heating said cobalt silicide layer 14 and said impurity diffused layers 9 and 10 with the 2nd temperature said Co2Si or CoSi -- CoSi2 While making it change, it solves by the manufacture approach of the semiconductor device characterized by having the process which forms said cobalt silicide layer 14 more deeply than the same depth as said amorphous layer 11, or said amorphous layer 11.
[0011] In the manufacture approach of the above-mentioned semiconductor device, it is characterized by said 1st temperature being 450 degrees C or less. In the manufacture approach of the above-mentioned semiconductor device, said 2nd temperature is characterized by being lower than the temperature in the case of said heat treatment which is 500 degrees C or more and forms an impurity diffused layer. In the manufacture approach of the above-mentioned semiconductor device, it is characterized by forming said cobalt film in the thickness of 8-20nm.
[0012] In the manufacture approach of the above-mentioned semiconductor device, after forming said cobalt film, before performing said heat treatment, it is characterized by having the process which forms cobalt and the cap layer (for example, TiN) which does not react on said cobalt film. In the manufacture approach of the above-mentioned semiconductor device, said element is characterized by being germanium, silicon, and arsenic. In this case, said germanium is 8x1013 atoms/cm2. An ion implantation is carried out above, the ion implantation of said silicon is carried out by two or more 8x1014 atoms/cm, and said arsenic is 8x1013 atoms/cm2 - 5x1014 atoms/cm2. It is characterized by carrying out an ion implantation.
[0013] (Operation) Next, an operation of this invention is explained. In order to form a cobalt silicide layer in the management of an impurity diffused layer according to this invention An amorphous layer is formed in the management of an impurity diffused layer which consists of silicon by the ion implantation. After forming the cobalt film on an impurity diffused layer

furthermore, the cobalt film and the silicon in an impurity diffused layer are made to react by 1st heat treatment, and they are CoSi or Co2Si at low temperature to the management of the amorphous layer. The becoming cobalt silicide layer is formed. Then, CoSi or Co2Si which removes the unreacted cobalt film and subsequently constitutes a cobalt silicide layer by 2nd heat treatment CoSi2 While making it change and forming sheet resistance into low resistance It is the same as the depth of an early amorphous layer, or the cobalt silicide layer is made to enter more deeply than it.

[0014] According to such a process, migration in the lower part of the configuration element of a cobalt silicide layer is barred by the amorphous layer in the case of the 1st heat treatment for forming a cobalt silicide layer, and the 2nd heat treatment, and generating of a spike of a cobalt silicide layer is prevented. And since it was made for the recrystallization to make it immersed by the cobalt silicide layer even if it extended the cobalt silicide layer to the depth in early stages of an amorphous layer and the amorphous layer recrystallized on the occasion of the 2nd heat treatment, junction in high recrystallization of resistance and a cobalt silicide layer is barred, and the rise of contact resistance is prevented.

[0015] If the temperature of the 1st heat treatment becomes 450 degrees C or more, since an amorphous layer recrystallizes from the bottom, the semantics made amorphous is lost. Moreover, if it is beyond temperature for the temperature of the 2nd heat treatment to activate an impurity diffused layer, since cobalt begins to melt from a silicide layer and junction leak is increased, it is not desirable. Such a cobalt silicide layer is used for the source layer of an MOS transistor, a drain layer, etc., and forms those layers into low resistance.

[0016] In addition, although especially the element that carries out an ion implantation in order to form an amorphous layer is not limited, germanium with big mass, silicon, its arsenic used for a dopant are desirable.

[0017]

[Embodiment of the Invention] Then, the operation gestalt of this invention is explained based on a drawing below. Below, the gestalt of operation of this invention is explained. Drawing 1 is the sectional view showing the process of 1 operation gestalt of this invention. First, drawing 1 (a) It is LOCOS among the silicon machine hills 1 so that it may be shown. The front face of the field separated with the oxide film 2 is oxidized thermally, and it is 5nm in thickness by this. The gate oxide 3 of extent is formed. Then, gate oxide 3 and LOCOS It is 150nm by the CVD method on an oxide film 2. The polish recon film 4 of the thickness of extent is formed.

[0018] Next, drawing 1 (b) After carrying out the ion implantation of the arsenic into the polish recon film 4 so that it may be shown, patterning of the polish recon film 4 and the gate oxide 3 is carried out, and the gate electrode 5 is formed with the polish recon film 4. The ion implantation of the arsenic is carried out to a mask at a silicon substrate 1, using the gate electrode 5, and the shallow impurity impregnation layer 6 is formed next. the dose of the ion implantation -- 3x1014 atm/cm2 it is -- the acceleration energy -- 10keV(s) it is .

[0019] Next, it is 100nm by the CVD method. The silicon oxide of the thickness of extent is formed. Then, anisotropic etching of the silicon oxide is perpendicularly carried out until the top face of the gate electrode 5 is exposed, and it is drawing 1 (c). It leaves silicon oxide to the side face of the gate electrode 5 as a sidewall 7 so that it may be shown. After that, the ion implantation of the arsenic is carried out to a mask at a silicon substrate 1 using the gate electrode 5, and the deep impurity impregnation layer 8 is formed. the dose of the ion implantation -- 2x1015 atm/cm2 it is -- the acceleration energy -- 40keV(s) it is .

[0020] Next, while making the interior diffuse the arsenic in the gate electrode 5 by RTA processing for 10 seconds at 1000 degrees C, the arsenic of the shallow impurity impregnation layer 6 and the deep impurity impregnation layer 8 is activated, and it is drawing 1 (d). The source layer 9 and the drain layer 10 of LDD structure as shown are formed in the silicon substrate 1 of the both sides of the gate electrode 5. In this case, the depth of the field which does not lap with a sidewall 7 among the source layer 9 and the drain layer 10 is set to about 100nm from the front face of a silicon substrate 1.

[0021] After that, it is drawing 1 (e). The ion implantation of the germanium is carried out to the whole containing the source layer 9 and the drain layer 10, and this forms the amorphous

(amorphous) layer 11 in the surface of the gate electrode 5, the source layer 9, and the drain layer 10 so that it may be shown. The ion implantation is dose 8x1013 atm/cm2. It is above. Moreover, the amorphous layer 11 is formed more shallowly than the bottom of the source layer 9 and the drain layer 10, and the acceleration energy at the time of an ion implantation is deep to extent to which the amorphous layer 11 moreover does not disappear at the time of the 1st next heat-treatment for silicide-izing, and is set as the magnitude in which the amorphous layer 11 disappears further at the time of the 2nd heat-treatment for silicide-izing.

[0022] Although specifically based on the depth of the silicide layer which it is going to form from now on, when the depth of the source layer 9 and the drain layer 10 is 100nm, it is 20-40keV. It is within the limits of extent. then, buffered fluoric acid -- the gate electrode 5, the source layer 9, and the drain layer 10 -- the silicon oxide of each front face is removed. Buffered fluoric acid is the mixed liquor of the rate of 100 about 2 and water in fluoric acid, and the removal time amount is about 60 seconds.

[0023] Next, drawing 2 (a) Sequential formation of the cobalt (Co) film 12 with a thickness of about 8-20nm and the about 30nm titanium nitride (TiN) film 13 is carried out by the spatter at the whole so that it may be shown. On the occasion of growth of the cobalt film 12, direct-current electric energy which impresses the argon quantity of gas flow to 5mTorr(s) and a growth ambient atmosphere to 100sccm(s) and a cobalt target for the growth ambient pressure force was made into 0.2 W/cm2. Thickness of the cobalt film 12 is made so thick that germanium ion-implantation energy is enlarged.

[0024] Moreover, on the occasion of growth of the titanium nitride film 13, direct-current electric energy which impresses the argon quantity of gas flow to 5mTorr(s) and a growth ambient atmosphere to 50sccm(s), and impresses a nitrogen quantity of gas flow to 50sccm(s) and a titanium nitride target for the growth ambient pressure force was made into 7.0 W/cm2. The titanium nitride film 13 is formed in order to control that irregularity arises on the front face of a silicide layer in the case of silicide-izing.

[0025] After that, the 1st above-mentioned heat-treatment for silicide-izing is performed. That is, if RTA (rapid thermal annealling) processing for 30 seconds is performed at 400-450 degrees C and each front face of the gate electrode 5, the source layer 9, and the drain layer 10 is silicide-ized in the ambient atmosphere of nitrogen or an argon as shown in drawing 2 (b), it is Co2Si to the upper part of the amorphous layer 11. Or the cobalt silicide layer 14 which consists of CoSi is formed. In addition, since it recrystallizes the bottom of the amorphous layer 11 when the cobalt silicide layer 14 will not be formed if RTA temperature becomes lower than 400 degrees C, and it becomes higher than 450 degrees C, it is not desirable. Since the ion-implantation energy of germanium is optimized as described above, the amorphous layer 11 did not disappear in this phase, and although the upper part of the amorphous layer 11 not only corrodes by the cobalt silicide layer 14, but single-crystal-izes from a bottom among the amorphous layers 11 at the time of this heat-treatment, even when it is small, it remains.

[0026] Next, drawing 2 (c) Mixed liquor of the hydrogen peroxide heated at 70 degrees C so that it might be shown, and aqueous ammonia (H2O2:NH4 OH:H2O =1:1:4) By soaking for 180 seconds, the titanium nitride film 13 is removed and continued and it is the mixed liquor (H2SO4:H2O2 =3:1) of a sulfuric acid and a hydrogen peroxide. The unreacted cobalt film 12 is removed by soaking for 20 minutes. In this case, the cobalt silicide layer 14 remains as it is.

[0027] Next, 2nd heat-treatment for silicide-izing is performed. Namely, drawing 2 (d) The cobalt silicide layer 14 is heated in a 600 degrees C - 900 degrees C temperature requirement in the ambient atmosphere of nitrogen or an argon so that it may be shown. Thereby, the cobalt silicide layer 14 is Co2Si. Or CoSi to CoSi2 Low resistance is changed and formed. In this case, it is CoSi2 when whenever [stoving temperature] is made lower than 600 degrees C. It is hard coming to be generated and it becomes impossible to attain low resistance-ization. Moreover, if whenever [stoving temperature] becomes high from 900 degrees C or more, Co atom will begin to melt from the cobalt silicide layer 14, and junction leak will be increased.

[0028] The thickness of the cobalt silicide layer 14 obtained by this is 0.5-2.0, when thickness in which the impurity diffused layer which constitutes the source layer 9 and the drain layer 10 remained is set to 1. It becomes extent. To next, it is drawing 2 (e). Silicon oxide 15 with a

thickness of 700nm is formed in the whole with a CVD method so that it may be shown. Subsequently After carrying out patterning of the silicon oxide 15 and forming a contact hole on the gate electrode 5, the source layer 9, and the drain layer 10 The titanium film 16 of 20nm of thickness, the titanium nitride film 17 of 100nm of thickness, and the aluminum layer 18 of 500nm of thickness are formed. Patterning of these three layers 16-18 is carried out by the photolithography method, and the common gate drawer electrode 19, the source drawer electrode 20, and the drain drawer electrode 21 are formed.

[0029] In addition, although germanium was used in the above-mentioned explanation in order to form the amorphous layer 14, the ion implantation of other elements, such as silicon, arsenic, and boron, may be carried out. In addition, germanium and silicon are desirable when the mass of an element, control of the high impurity concentration of an impurity diffused layer, etc. are taken into consideration. The ion implantation of the germanium is carried out by two or more 8x1013 atoms/cm, the ion implantation of the silicon is carried out by two or more 8x1014 atoms/cm, and the ion implantation of the arsenic is carried out by 8x1013 atoms/cm2 - 5x1014 atoms/cm2.

[0030] At the pars basilaris ossis occipitalis of the cobalt silicide layer 14 in the MOS transistor formed of the above processes, a spike hardly occurred, but leakage current was controlled. Below, spike generating of the cobalt silicide layer 14 is explained in full detail. Drawing 3 (a) After forming the cobalt layer 12 of 10nm of thickness on it without making a silicon substrate 1 amorphous so that it may be shown, the 1st experiment as shown below was conducted.

[0031] First, drawing 3 (b) It is Co2Si, when the cobalt layer 12 and the silicon substrate 1 were heated at 400 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed in the surface of a silicon substrate 1. Next, drawing 3 (c) Co2Si which constituted the cobalt silicide layer 14 when the cobalt silicide layer 14 and the silicon substrate 1 were heated at 450 degrees C so that it might be shown It changed to CoSi. Then, drawing 3 (d) CoSi is CoSi2, when the cobalt silicide layer 14 was heated at 600 more degrees C so that it might be shown. It changed and, moreover, the spike 22 had arisen in the base of the cobalt silicide layer 14. CoSi2 after removing unreacted cobalt When TEM observation of the sectional view of the interface of Si was carried out, it came to be shown in drawing 4 , and the interface is irregular and abnormality growth (spike) of the shape of about 80nm icicle had produced it at the maximum.

[0032] Next, drawing 5 (a) After making a silicon substrate 1 amorphous shallowly from a front face so that it may be shown, the cobalt layer 12 of 10nm of thickness was formed on it, and the 2nd experiment as subsequently to a degree shown was conducted. First, drawing 5 (b) It is Co2Si, when the cobalt layer 12 and the silicon substrate 1 were heated at 400 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed in silicon substrate 1 surface, and the thin amorphous layer 11 remained in the pars basilaris ossis occipitalis. Next, it is drawing 5 (c). Co2Si which constitutes the cobalt silicide layer 14 when the cobalt layer 14 and silicon substrate 1 which were heated at 400 degrees C are heated at 450 more degrees C so that it may be shown It changed to CoSi and, moreover, the cobalt silicide layer 14 corroded the amorphous layer 11 altogether. And the spike had arisen in the base of the cobalt silicide layer 14. Furthermore, drawing 5 (d) It is CoSi2, when the cobalt silicide layer 14 was again heated at 600 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed and the spike 22 had arisen in the base.

[0033] Next, drawing 6 (a) After making the surface of a silicon substrate 1 amorphous deeply so that it may be shown, the cobalt layer 12 of 10nm of thickness was generated, and the 3rd experiment shown further below was conducted. First, drawing 6 (b) It is Co2Si, when the cobalt layer 12 and the silicon substrate 1 were heated at 400 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed in the surface of a silicon substrate 1, and the thick amorphous layer 11 remained in the pars basilaris ossis occipitalis. Then, drawing 6 (c) Co2Si which constitutes the cobalt silicide layer 14 when the cobalt silicide layer 14 and silicon substrate 1 which were heated at 400 degrees C are heated at 450 more degrees C so that it may be shown Although it changed to CoSi and the amorphous layer 11 existed in the lower part, the pars basilaris ossis occipitalis of the amorphous layer 11 was recrystallized slightly.

Furthermore, drawing 6 (d) It is CoSi2, when the cobalt silicide layer 14 was again heated at 600 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed, and spike 22 did not arise in the base, but, moreover, the silicon layer 23 of the result which the amorphous layer 11 recrystallized existed in the lower part.

[0034] Therefore, in order to prevent generating of the spike from the cobalt silicide layer 14, it is thought that what is necessary is just to make the amorphous layer 11 deep enough like the process of the 3rd experiment. As shown in drawing 2 in fact, a source layer and a drain layer exist in the silicon layer 23 which recrystallized, and whenever [stoving temperature / of about 850 degrees C] is not enough as activation of the impurity in the amorphous layer 11, and it becomes impossible however, for contact resistance with the cobalt silicide layer 14, and a source layer / drain layer to fully reduce it. Thereby, the original purpose of silicide-izing called the reduction in resistance of a source layer and a drain layer cannot be attained.

[0035] Next, drawing 7 (a) After making the surface of a silicon substrate amorphous so that it may be shown, the cobalt layer 12 of 10nm of thickness was formed, and the 4th experiment shown below was conducted further. That is [it made the depth of the amorphous layer 11 into the proper value], it was made for the cobalt silicide layer 14 to also corrode the silicon layer 23 which the amorphous layer 11 existed under the cobalt silicide layer 14 after the 1st heat-treatment, and was recrystallized of the amorphous layers 11 in the reheating processing which is 600 degrees C in this experiment.

[0036] First, drawing 7 (b) It is Co2Si, when the cobalt layer 12 and the silicon substrate 1 were heated for 30 seconds at 400 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed in silicon substrate 1 surface, and the amorphous layer 11 remained in the lower part. Then, drawing 7 (c) Co2Si which constitutes the cobalt silicide layer 14 when the cobalt silicide layer 14 and a silicon substrate 1 are heated for 30 seconds at 450 more degrees C so that it may be shown It changed to CoSi. Moreover, thickness is 20.2nm and the cobalt silicide layer 14 changed into the condition that 2.0mm projected from the front face of a silicon substrate 1, among those. Moreover, the silicon layer 23 and the amorphous layer 11 which were recrystallized under the cobalt silicide layer 14 existed, and such thickness was 18.2nm or less in total.

[0037] Furthermore, drawing 7 (d) CoSi which constituted the cobalt silicide layer 14 when the cobalt silicide layer 14 and the silicon substrate 1 were reheated for 30 seconds at 600 degrees C so that it might be shown is CoSi2. It became and thickness became thick with 35.2nm. In this case, since 1.2nm of cobalt silicide layers 14 sank and they existed from the front face of a silicon substrate 1, the amorphous layer 14 of the beginning was completely corroded in the cobalt silicide layer 14, and, moreover, the silicon layer 23 which recrystallized did not exist in that lower part.

[0038] Therefore, the condition of low resistance that the source layer and drain layer which exist under the cobalt silicide layer 14 were first activated at about 1000 degrees C has been maintained, and, thereby, contact resistance with the cobalt silicide layer 14, and a source layer and a drain layer was good. Moreover, CoSi2 When TEM observation of the interface of Si was carried out, abnormality growth like drawing 4 was not seen, but the interface was comparatively flat.

[0039] From the above thing, the cobalt film of 10nm - 20nm of thickness is formed. This by the 1st time The temperature of 400 degrees C - 450 degrees C, It heats for 30 seconds at the temperature of 600-900 degrees C by the 2nd time, respectively, and is CoSi2. In forming the cobalt silicide layer 14 It turned out that it is necessary to form the amorphous layer 11 so that it may become about 18.2nm - 26.4nm or more a depth of 35.2nm - 70.2nm or less to each thickness.

[0040] Moreover, Co2Si Or when forming the silicide layer 14 which consists of CoSi, it is effective if it carries out on the temperature conditions which a silicide reaction occurs and make the recrystallization rate of the amorphous layer 11 extremely late. For example, as shown in drawing 8 , the recrystallization rate of the amorphous layer 11 becomes extremely slow below 450 degrees C. Moreover, when forming the amorphous layer 11, it turns out that the direction in the case of containing an impurity has a recrystallization rate slower than the case where an

impurity is not contained.
[0041] Finally, the leakage current of a cobalt silicide layer is explained. As shown in drawing 9, while leakage current grounded the silicon substrate 31, it impressed the forward electrical potential difference to the cobalt silicide layer 33 of the management of an impurity diffused layer 32. First, the case where the ion implantation of the germanium is not carried out is explained. Immediately after [forming the cobalt silicide layer 33 and removing unreacted cobalt after that by 550 degrees C and 1st RTA for 30 seconds,], Namely, the relation of the leakage current and bias voltage just behind a washout The place which changed and investigated the plane area of an impurity diffused layer 32 about (it is hereafter called a leak current characteristic), Drawing 10 (a) - (c) When the result as shown was obtained and the circumference length of an impurity diffused layer 32 was changed and investigated about the leak current characteristic, it is drawing 11 (a). - (c) The result as shown was obtained.
[0042] Furthermore, it is CoSi2 by 825 degrees C and 2nd RTA for 30 seconds. The place which changed and investigated the area of an impurity diffused layer 32 about the leak current characteristic after forming the becoming cobalt silicide layer 33, drawing 12 (a) - (c) the place which the result as shown was obtained, and changed and investigated the circumference length of an impurity diffused layer 32 about the leak current characteristic -- drawing 13 (a) and (b) The result as shown was obtained.
[0043] According to drawing 10 - drawing 13 , the leak current characteristic after 1st RTA has deteriorated, so that it is bad and circumference length becomes [the area of an impurity diffused layer 32] larger than the leak current characteristic of 2nd RTA for a long time. This is based on the spike of the pars basilaris ossis occipitalis of the cobalt silicide layer 33. Next, the case where poured in germanium and the management of an impurity diffused layer 32 is beforehand made amorphous is explained.
[0044] When the plane area of an impurity diffused layer 32 was changed and investigated about the leak current characteristic just behind a washout through 550 degrees C and 1st RTA for 30 seconds, it is drawing 14 R> 4 (a). - (c) When the result as shown was obtained and the circumference length of an impurity diffused layer 32 was changed and investigated about the leak current characteristic, it is drawing 15 (a). - (c) The result as shown was obtained.
[0045] Furthermore, it is CoSi2 by 825 degrees C and 2nd RTA for 30 seconds. The place which changed and investigated the area of an impurity diffused layer 32 about the leak current characteristic after forming the becoming cobalt silicide layer 33, drawing 16 (a) - (c) the place which the result as shown was obtained, and changed and investigated the circumference length of an impurity diffused layer 32 about the leak current characteristic -- drawing 17 (a) and (b) The result as shown was obtained.
[0046] According to drawing 14 - drawing 17 , when it is made amorphous by the ion implantation of germanium, there is little variation in a leak current characteristic, and, moreover, most of the area of an impurity diffused layer 32 and the dependency of circumference length is not seen. Next, the result investigated about the cobalt thickness dependency of the leak current characteristic of the cobalt silicide layer 33 after 2nd RTA is shown in drawing 18 R> 8 and drawing 19 .
[0047] If the case where an ion implantation is carried out to the case where the ion implantation of the germanium is not carried out when the cobalt film is 10nm is compared from drawing 18 and 19, among them, a difference will hardly be seen about a leak current characteristic, but when the cobalt film is thickened with 18nm, it turns out that a clearly good leak current characteristic is acquired for the direction at the time of carrying out the ion implantation of the germanium.
[0048] In addition, although the sheet resistance of the cobalt silicide layer at the time of forming a cobalt silicide layer, having used thickness of the cobalt film as 18nm was investigated, they were about 4ohm/** irrespective of the existence of a germanium ion implantation. When the ion implantation of the germanium is carried out and it is made amorphous to a silicon substrate also by the above experimental result before forming the cobalt film, it turns out that few good junction properties of the area dependency of an impurity diffused layer, a circumference length dependency, and a cobalt thickness dependency are acquired.

[0049]
[Effect of the Invention] As stated above, in order to form a cobalt silicide layer in the management of an impurity diffused layer according to this invention After forming an amorphous layer in the management of an impurity diffused layer which consists of silicon by the ion implantation After forming the cobalt film on an impurity diffused layer, the cobalt film and the silicon in an impurity diffused layer are made to react by 1st heat treatment, and they are CoSi or Co2Si at low temperature to the management of the amorphous layer. Form the becoming cobalt silicide layer, and the unreacted cobalt film is removed continuously. Subsequently, CoSi or Co2Si which constitutes a cobalt silicide layer by 2nd heat treatment CoSi2 While making it change and forming low resistance By that of ** which is the same as an early amorphous layer, or is made to enter more deeply than it, a cobalt silicide layer In the case of the 1st heat treatment for forming a cobalt silicide layer, and the 2nd heat treatment, migration in the lower part of the configuration element of a cobalt silicide layer is barred by the amorphous layer, and generating of a spike of a cobalt silicide layer can be prevented. And since a cobalt silicide layer is immersed in the recrystallization even if it extends a cobalt silicide layer to the depth in early stages of an amorphous layer and an amorphous layer recrystallizes in the case of the 2nd heat treatment, junction in high recrystallization of resistance and a cobalt silicide layer is barred, and it can prevent that contact resistance goes up.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the manufacture approach of a semiconductor device of having a salicide process, in more detail about the manufacture approach of a semiconductor device.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] High integration of today's semiconductor device and speed-izing of high-speed-izing can be remarkable, and can enjoy now easily a high-speed three-dimension image processing, a high-speed communication link, etc. with a domestic personal computer and a domestic game machine. Such high performance-ization has been realized by only making size of a CMOS device detailed. The present CMOS device is in the mass-production phase of magnitude where gate length is about 0.35 micrometers, and the 0.1 -0.05micrometer CMOS device is also reported by research level. However, the parasitism resistance according to a scaling law becomes large, and the engine performance does not go up as the conventional trend by the device with which gate length becomes smaller than 0.35 micrometers. Then, the process which silicide-izes the gate, the source, and a drain to coincidence, and forms them into low resistance to it, i.e., a salicide process, is an indispensable technique.
[0003] In the MOS transistor, if a diffusion layer is made shallow in order to suppress the short channel effect etc., since increase of resistance of a diffusion layer will be brought about, the technique which silicide-izes the polish recon front face which constitutes a gate electrode, and the front face of a source layer and a drain layer in self align, and forms them into low resistance is examined. As the silicide, ingredients, such as TiSi2, CoSi2, and NiSi, are used.
[0004] Next, the general production process of the MOS transistor which used Co Salicide for the surface of the gate, the source, and a drain is explained. First, drawing 20 (a) It is the silicon machine hill 101 so that it may be shown. It is LOCOS inside. Oxide film 102 It is about 50A gate oxide 103 by thermal oxidation about the front face of the separated field. It forms. Then, it is the polish recon film 104 of about 1500A thickness by the CVD method on it. It forms.
[0005] Next, drawing 20 (b) It is the polish recon film 104 so that it may be shown. After carrying out the ion implantation of either PORON, Lynn or arsenic inside, it is the polish recon film 104. Patterning is carried out and it is the gate electrode 105. It forms. The ion implantation of the next door is carried out next, and it is the shallow impurity impregnation layer 106. It forms. next, drawing 20 (c) it is shown -- as -- a CVD method -- silicon oxide with a thickness of about 1000A -- forming -- gate electrode 105 until it exposes -- anisotropic etching -- carrying out -- silicon oxide -- sidewall 107 ****** -- it leaves.
[0006] After that, the ion implantation of the next door is carried out, and it is the deep impurity impregnation layer 108. Impurity impregnation layer 106 shallow after forming Deep impurity impregnation layer 108 It is activated by heat-treatment and, thereby, is the gate electrode 105. Silicon substrate 101 of both sides Source layer 109 of LDD structure Drain layer 110 It will form. next, buffered fluoric acid -- the gate electrode 105, the source layer 109, and drain layer 110 after removing the silicon oxide (natural oxidation film) of each front face -- drawing 20 (d) it is shown -- as -- About 100A cobalt film 111 About 300A titanium nitride film 112 forming -- RTA for 550 ** 30 seconds (rapid thermal annealling) processing -- silicide ---izing -- cobalt silicide layer 113 It forms.
[0007] Then, drawing 20 (e) It is the titanium nitride film 112 so that it may be shown. The unreacted cobalt film 111 is removed and it is RTA for further 850 **30 seconds. It processes and, thereby, they are the gate electrode 105 and the source layer 109. And drain layer 110 The cobalt silicide layer 114 formed in the front face is further formed into low resistance. Such a

Salicide technique is a fundamental process, as the amelioration technique, the flattening technique of a silicide layer is shown in JP,62-33466,A, and the equalization technique of the thickness of a silicide layer is indicated by JP,5-291180,A.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] As stated above, in order to form a cobalt silicide layer in the management of an impurity diffused layer according to this invention After forming an amorphous layer in the management of an impurity diffused layer which consists of silicon by the ion implantation After forming the cobalt film on an impurity diffused layer, the cobalt film and the silicon in an impurity diffused layer are made to react by 1st heat treatment, and they are CoSi or Co2Si at low temperature to the management of the amorphous layer. Form the becoming cobalt silicide layer, and the unreacted cobalt film is removed continuously. Subsequently, CoSi or Co2Si which constitutes a cobalt silicide layer by 2nd heat treatment CoSi2 While making it change and forming low resistance By that of ** which is the same as an early amorphous layer, or is made to enter more deeply than it, a cobalt silicide layer In the case of the 1st heat treatment for forming a cobalt silicide layer, and the 2nd heat treatment, migration in the lower part of the configuration element of a cobalt silicide layer is barred by the amorphous layer, and generating of a spike of a cobalt silicide layer can be prevented. And since a cobalt silicide layer is immersed in the recrystallization even if it extends a cobalt silicide layer to the depth in early stages of an amorphous layer and an amorphous layer recrystallizes in the case of the 2nd heat treatment, junction in high recrystallization of resistance and a cobalt silicide layer is barred, and it can prevent that contact resistance goes up.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] When formation of the above cobalt silicide layers has a source layer and a deep drain layer, there is especially no problem, but when it becomes shallow, for example to about 100nm, there is a problem that leakage current becomes easy to flow. It thinks for the spike of cobalt silicide occurring from the bottom of a cobalt silicide layer, and running through a source layer and a drain layer as the cause. The spike of such cobalt silicide was produced even if formed according to the approach and temperature conditions which were indicated by two patent official reports which described the cobalt silicide layer above.
[0009] This invention is made in view of such a problem, and aims at offering the manufacture approach of a semiconductor device including the process which forms the cobalt silicide layer which a spike cannot produce easily on a base.

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MEANS

[Means for Solving the Problem]

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OPERATION

(Operation) Next, an operation of this invention is explained. In order to form a cobalt silicide layer in the management of an impurity diffused layer according to this invention An amorphous layer is formed in the management of an impurity diffused layer which consists of silicon by the ion implantation. After forming the cobalt film on an impurity diffused layer furthermore, the cobalt film and the silicon in an impurity diffused layer are made to react by 1st heat treatment, and they are CoSi or Co2Si at low temperature to the management of the amorphous layer. The becoming cobalt silicide layer is formed. Then, CoSi or Co2Si which removes the unreacted cobalt film and subsequently constitutes a cobalt silicide layer by 2nd heat treatment CoSi2 While making it change and forming sheet resistance into low resistance It is the same as the depth of an early amorphous layer, or the cobalt silicide layer is made to enter more deeply than it.
[0014] According to such a process, migration in the lower part of the configuration element of a cobalt silicide layer is barred by the amorphous layer in the case of the 1st heat treatment for forming a cobalt silicide layer, and the 2nd heat treatment, and generating of a spike of a cobalt silicide layer is prevented. And since it was made for the recrystallization to make it immersed by the cobalt silicide layer even if it extended the cobalt silicide layer to the depth in early stages of an amorphous layer and the amorphous layer recrystallized on the occasion of the 2nd heat treatment, junction in high recrystallization of resistance and a cobalt silicide layer is barred, and the rise of contact resistance is prevented.
[0015] If the temperature of the 1st heat treatment becomes 450 degrees C or more, since an amorphous layer recrystallizes from the bottom, the semantics made amorphous is lost. Moreover, if it is beyond temperature for the temperature of the 2nd heat treatment to activate an impurity diffused layer, since cobalt begins to melt from a silicide layer and junction leak is increased, it is not desirable. Such a cobalt silicide layer is used for the source layer of an MOS transistor, a drain layer, etc., and forms those layers into low resistance.
[0016] In addition, although especially the element that carries out an ion implantation in order to form an amorphous layer is not limited, germanium with big mass, silicon, its arsenic used for a dopant are desirable.
[0017]
[Embodiment of the Invention] Then, the operation gestalt of this invention is explained based on a drawing below. Below, the gestalt of operation of this invention is explained. Drawing 1 is the sectional view showing the process of 1 operation gestalt of this invention. First, drawing 1 (a) It is LOCOS among the silicon machine hills 1 so that it may be shown. The front face of the field separated with the oxide film 2 is oxidized thermally, and it is 5nm in thickness by this. The gate oxide 3 of extent is formed. Then, gate oxide 3 and LOCOS It is 150nm by the CVD method on an oxide film 2. The polish recon film 4 of the thickness of extent is formed.
[0018] Next, drawing 1 (b) After carrying out the ion implantation of the arsenic into the polish recon film 4 so that it may be shown, patterning of the polish recon film 4 and the gate oxide 3 is carried out, and the gate electrode 5 is formed with the polish recon film 4. The ion implantation of the arsenic is carried out to a mask at a silicon substrate 1, using the gate electrode 5, and the shallow impurity impregnation layer 6 is formed next. the dose of the ion implantation --

3x1014 atm/cm2 it is -- the acceleration energy -- 10keV(s) it is .
[0019] Next, it is 100nm by the CVD method. The silicon oxide of the thickness of extent is formed. Then, anisotropic etching of the silicon oxide is perpendicularly carried out until the top face of the gate electrode 5 is exposed, and it is drawing 1 (c). It leaves silicon oxide to the side face of the gate electrode 5 as a sidewall 7 so that it may be shown. After that, the ion implantation of the arsenic is carried out to a mask at a silicon substrate 1 using the gate electrode 5, and the deep impurity impregnation layer 8 is formed. the dose of the ion implantation -- 2x1015 atm/cm2 it is -- the acceleration energy -- 40keV(s) it is .
[0020] Next, while making the interior diffuse the arsenic in the gate electrode 5 by RTA processing for 10 seconds at 1000 degrees C, the arsenic of the shallow impurity impregnation layer 6 and the deep impurity impregnation layer 8 is activated, and it is drawing 1 (d). The source layer 9 and the drain layer 10 of LDD structure as shown are formed in the silicon substrate 1 of the both sides of the gate electrode 5. In this case, the depth of the field which does not lap with a sidewall 7 among the source layer 9 and the drain layer 10 is set to about 100nm from the front face of a silicon substrate 1.
[0021] After that, it is drawing 1 (e). The ion implantation of the germanium is carried out to the whole containing the source layer 9 and the drain layer 10, and this forms the amorphous (amorphous) layer 11 in the surface of the gate electrode 5, the source layer 9, and the drain layer 10 so that it may be shown. The ion implantation is dose 8x1013 atm/cm2. It is above. Moreover, the amorphous layer 11 is formed more shallowly than the bottom of the source layer 9 and the drain layer 10, and the acceleration energy at the time of an ion implantation is deep to extent to which the amorphous layer 11 moreover does not disappear at the time of the 1st next heat-treatment for silicide-izing, and is set as the magnitude in which the amorphous layer 11 disappears further at the time of the 2nd heat-treatment for silicide-izing.
[0022] Although specifically based on the depth of the silicide layer which it is going to form from now on, when the depth of the source layer 9 and the drain layer 10 is 100nm, it is 20-40keV. It is within the limits of extent. then, buffered fluoric acid -- the gate electrode 5, the source layer 9, and the drain layer 10 -- the silicon oxide of each front face is removed. Buffered fluoric acid is the mixed liquor of the rate of 100 about 2 and water in fluoric acid, and the removal time amount is about 60 seconds.
[0023] Next, drawing 2 (a) Sequential formation of the cobalt (Co) film 12 with a thickness of about 8-20nm and the about 30nm titanium nitride (TiN) film 13 is carried out by the spatter at the whole so that it may be shown. On the occasion of growth of the cobalt film 12, direct-current electric energy which impresses the argon quantity of gas flow to 5mTorr(s) and a growth ambient atmosphere to 100sccm(s) and a cobalt target for the growth ambient pressure force was made into 0.2 W/cm2. Thickness of the cobalt film 12 is made so thick that germanium ion-implantation energy is enlarged.
[0024] Moreover, on the occasion of growth of the titanium nitride film 13, direct-current electric energy which impresses the argon quantity of gas flow to 5mTorr(s) and a growth ambient atmosphere to 50sccm(s), and impresses a nitrogen quantity of gas flow to 50sccm(s) and a titanium nitride target for the growth ambient pressure force was made into 7.0 W/cm2. The titanium nitride film 13 is formed in order to control that irregularity arises on the front face of a silicide layer in the case of silicide-izing.
[0025] After that, the 1st above-mentioned heat-treatment for silicide-izing is performed. That is, if RTA (rapid thermal annealling) processing for 30 seconds is performed at 400-450 degrees C and each front face of the gate electrode 5, the source layer 9, and the drain layer 10 is silicide-ized in the ambient atmosphere of nitrogen or an argon as shown in drawing 2 (b), it is Co2Si to the upper part of the amorphous layer 11. Or the cobalt silicide layer 14 which consists of CoSi is formed. In addition, since it recrystallizes the bottom of the amorphous layer 11 when the cobalt silicide layer 14 will not be formed if RTA temperature becomes lower than 400 degrees C, and it becomes higher than 450 degrees C, it is not desirable. Since the ion-implantation energy of germanium is optimized as described above, the amorphous layer 11 did not disappear in this phase, and although the upper part of the amorphous layer 11 not only corrodes by the cobalt silicide layer 14, but single-crystal-izes from a bottom among the

the time of this heat-treatment, even when it is small, it remains.
c) Mixed liquor of the hydrogen peroxide heated at 70 degrees C so that
iqueous ammonia (H2O2:NH4 OH:H2O =1:1:4) By soaking for 180
tride film 13 is removed and continued and it is the mixed liquor
sulfuric acid and a hydrogen peroxide. The unreacted cobalt film 12 is
20 minutes. In this case, the cobalt silicide layer 14 remains as it is.
reatment for silicide-izing is performed. Namely, drawing 2 (d) The cobalt
d in a 600 degrees C - 900 degrees C temperature requirement in the
nitrogen or an argon so that it may be shown. Thereby, the cobalt silicide
Si to CoSi2 Low resistance is changed and formed. In this case, it is
stoving temperature] is made lower than 600 degrees C. It is hard
and it becomes impossible to attain low resistance-ization. Moreover, if
erature] becomes high from 900 degrees C or more, Co atom will begin
silicide layer 14, and junction leak will be increased.
the cobalt silicide layer 14 obtained by this is 0.5-2.0, when thickness in
ed layer which constitutes the source layer 9 and the drain layer 10
ecomes extent. To next, it is drawing 2 (e). Silicon oxide 15 with a
rmed in the whole with a CVD method so that it may be shown.
ying out patterning of the silicon oxide 15 and forming a contact hole on
e source layer 9, and the drain layer 10 The titanium film 16 of 20nm of
itride film 17 of 100nm of thickness, and the aluminum layer 18 of 500nm
. Patterning of these three layers 16-18 is carried out by the
d, and the common gate drawer electrode 19, the source drawer
ain drawer electrode 21 are formed.
ugh germanium was used in the above-mentioned explanation in order to
er 14, the ion implantation of other elements, such as silicon, arsenic, and
ut. In addition, germanium and silicon are desirable when the mass of an
high impurity concentration of an impurity diffused layer, etc. are taken
ion implantation of the germanium is carried out by two or more 8x1013
ntation of the silicon is carried out by two or more 8x1014 atoms/cm,
of the arsenic is carried out by 8x1013 atoms/cm2 - 5x1014

aris ossis occipitalis of the cobalt silicide layer 14 in the MOS transistor
cesses, a spike hardly occurred, but leakage current was controlled.
of the cobalt silicide layer 14 is explained in full detail. Drawing 3 (a)
: layer 12 of 10nm of thickness on it without making a silicon substrate 1
ay be shown, the 1st experiment as shown below was conducted.
b) It is Co2Si, when the cobalt layer 12 and the silicon substrate 1 were
C so that it might be shown. The cobalt silicide layer 14 shown was
f a silicon substrate 1. Next, drawing 3 (c) Co2Si which constituted the
vhen the cobalt silicide layer 14 and the silicon substrate 1 were heated
at it might be shown It changed to CoSi. Then, drawing 3 (d) CoSi is
silicide layer 14 was heated at 600 more degrees C so that it might be
moreover, the spike 22 had arisen in the base of the cobalt silicide layer
g unreacted cobalt When TEM observation of the sectional view of the
ied out, it came to be shown in drawing 4 , and the interface is irregular
(spike) of the shape of about 80nm icicle had produced it at the

a) After making a silicon substrate 1 amorphous shallowly from a front
hown, the cobalt layer 12 of 10nm of thickness was formed on it, and the
equently to a degree shown was conducted. First, drawing 5 (b) It is
layer 12 and the silicon substrate 1 were heated at 400 degrees C so
The cobalt silicide layer 14 shown was formed in silicon substrate 1
norphous layer 11 remained in the pars basilaris ossis occipitalis. Next, it

is drawing 5 (c). Co2Si which constitutes the cobalt silicide layer 14 when the cobalt layer 14 and silicon substrate 1 which were heated at 400 degrees C are heated at 450 more degrees C so that it may be shown It changed to CoSi and, moreover, the cobalt silicide layer 14 corroded the amorphous layer 11 altogether. And the spike had arisen in the base of the cobalt silicide layer 14. Furthermore, drawing 5 (d) It is CoSi2, when the cobalt silicide layer 14 was again heated at 600 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed and the spike 22 had arisen in the base.

[0033] Next, drawing 6 (a) After making the surface of a silicon substrate 1 amorphous deeply so that it may be shown, the cobalt layer 12 of 10nm of thickness was generated, and the 3rd experiment shown further below was conducted. First, drawing 6 (b) It is Co2Si, when the cobalt layer 12 and the silicon substrate 1 were heated at 400 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed in the surface of a silicon substrate 1, and the thick amorphous layer 11 remained in the pars basilaris ossis occipitalis. Then, drawing 6 (c) Co2Si which constitutes the cobalt silicide layer 14 when the cobalt silicide layer 14 and silicon substrate 1 which were heated at 400 degrees C are heated at 450 more degrees C so that it may be shown Although it changed to CoSi and the amorphous layer 11 existed in the lower part, the pars basilaris ossis occipitalis of the amorphous layer 11 was recrystallized slightly. Furthermore, drawing 6 (d) It is CoSi2, when the cobalt silicide layer 14 was again heated at 600 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed, and spike 22 did not arise in the base, but, moreover, the silicon layer 23 of the result which the amorphous layer 11 recrystallized existed in the lower part.

[0034] Therefore, in order to prevent generating of the spike from the cobalt silicide layer 14, it is thought that what is necessary is just to make the amorphous layer 11 deep enough like the process of the 3rd experiment. As shown in drawing 2 in fact, a source layer and a drain layer exist in the silicon layer 23 which recrystallized, and whenever [stoving temperature / of about 850 degrees C] is not enough as activation of the impurity in the amorphous layer 11, and it becomes impossible however, for contact resistance with the cobalt silicide layer 14, and a source layer / drain layer to fully reduce it. Thereby, the original purpose of silicide-izing called the reduction in resistance of a source layer and a drain layer cannot be attained.

[0035] Next, drawing 7 (a) After making the surface of a silicon substrate amorphous so that it may be shown, the cobalt layer 12 of 10nm of thickness was formed, and the 4th experiment shown below was conducted further. That is [it made the depth of the amorphous layer 11 into the proper value], it was made for the cobalt silicide layer 14 to also corrode the silicon layer 23 which the amorphous layer 11 existed under the cobalt silicide layer 14 after the 1st heat-treatment, and was recrystallized of the amorphous layers 11 in the reheating processing which is 600 degrees C in this experiment.

[0036] First, drawing 7 (b) It is Co2Si, when the cobalt layer 12 and the silicon substrate 1 were heated for 30 seconds at 400 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed in silicon substrate 1 surface, and the amorphous layer 11 remained in the lower part. Then, drawing 7 (c) Co2Si which constitutes the cobalt silicide layer 14 when the cobalt silicide layer 14 and a silicon substrate 1 are heated for 30 seconds at 450 more degrees C so that it may be shown It changed to CoSi. Moreover, thickness is 20.2nm and the cobalt silicide layer 14 changed into the condition that 2.0mm projected from the front face of a silicon substrate 1, among those. Moreover, the silicon layer 23 and the amorphous layer 11 which were recrystallized under the cobalt silicide layer 14 existed, and such thickness was 18.2nm or less in total.

[0037] Furthermore, drawing 7 (d) CoSi which constituted the cobalt silicide layer 14 when the cobalt silicide layer 14 and the silicon substrate 1 were reheated for 30 seconds at 600 degrees C so that it might be shown is CoSi2. It became and thickness became thick with 35.2nm. In this case, since 1.2nm of cobalt silicide layers 14 sank and they existed from the front face of a silicon substrate 1, the amorphous layer 14 of the beginning was completely corroded in the cobalt silicide layer 14, and, moreover, the silicon layer 23 which recrystallized did not exist in that lower part.

[0038] Therefore, the condition of low resistance that the source layer and drain layer which

exist under the cobalt silicide layer 14 were first activated at about 1000 degrees C has been maintained, and, thereby, contact resistance with the cobalt silicide layer 14, and a source layer and a drain layer was good. Moreover, CoSi2 When TEM observation of the interface of Si was carried out, abnormality growth like drawing 4 was not seen, but the interface was comparatively flat.

[0039] From the above thing, the cobalt film of 10nm - 20nm of thickness is formed. This by the 1st time The temperature of 400 degrees C - 450 degrees C, It heats for 30 seconds at the temperature of 600-900 degrees C by the 2nd time, respectively, and is CoSi2. In forming the cobalt silicide layer 14 It turned out that it is necessary to form the amorphous layer 11 so that it may become about 18.2nm - 26.4nm or more a depth of 35.2nm - 70.2nm or less to each thickness.

[0040] Moreover, Co2Si Or when forming the silicide layer 14 which consists of CoSi, it is effective if it carries out on the temperature conditions which a silicide reaction occurs and make the recrystallization rate of the amorphous layer 11 extremely late. For example, as shown in drawing 8 , the recrystallization rate of the amorphous layer 11 becomes extremely slow below 450 degrees C. Moreover, when forming the amorphous layer 11, it turns out that the direction in the case of containing an impurity has a recrystallization rate slower than the case where an impurity is not contained.

[0041] Finally, the leakage current of a cobalt silicide layer is explained. As shown in drawing 9 , while leakage current grounded the silicon substrate 31, it impressed the forward electrical potential difference to the cobalt silicide layer 33 of the management of an impurity diffused layer 32. First, the case where the ion implantation of the germanium is not carried out is explained. Immediately after [forming the cobalt silicide layer 33 and removing unreacted cobalt after that by 550 degrees C and 1st RTA for 30 seconds,], Namely, the relation of the leakage current and bias voltage just behind a washout The place which changed and investigated the plane area of an impurity diffused layer 32 about (it is hereafter called a leak current characteristic), Drawing 10 (a) - (c) When the result as shown was obtained and the circumference length of an impurity diffused layer 32 was changed and investigated about the leak current characteristic, it is drawing 11 (a). - (c) The result as shown was obtained.

[0042] Furthermore, it is CoSi2 by 825 degrees C and 2nd RTA for 30 seconds. The place which changed and investigated the area of an impurity diffused layer 32 about the leak current characteristic after forming the becoming cobalt silicide layer 33, drawing 12 (a) - (c) the place which the result as shown was obtained, and changed and investigated the circumference length of an impurity diffused layer 32 about the leak current characteristic -- drawing 13 (a) and (b) The result as shown was obtained.

[0043] According to drawing 10 - drawing 13 , the leak current characteristic after 1st RTA has deteriorated, so that it is bad and circumference length becomes [the area of an impurity diffused layer 32] larger than the leak current characteristic of 2nd RTA for a long time. This is based on the spike of the pars basilaris ossis occipitalis of the cobalt silicide layer 33. Next, the case where poured in germanium and the management of an impurity diffused layer 32 is beforehand made amorphous is explained.

[0044] When the plane area of an impurity diffused layer 32 was changed and investigated about the leak current characteristic just behind a washout through 550 degrees C and 1st RTA for 30 seconds, it is drawing 14 R> 4 (a). - (c) When the result as shown was obtained and the circumference length of an impurity diffused layer 32 was changed and investigated about the leak current characteristic, it is drawing 15 (a). - (c) The result as shown was obtained.

[0045] Furthermore, it is CoSi2 by 825 degrees C and 2nd RTA for 30 seconds. The place which changed and investigated the area of an impurity diffused layer 32 about the leak current characteristic after forming the becoming cobalt silicide layer 33, drawing 16 (a) - (c) the place which the result as shown was obtained, and changed and investigated the circumference length of an impurity diffused layer 32 about the leak current characteristic -- drawing 17 (a) and (b) The result as shown was obtained.

[0046] According to drawing 14 - drawing 17 , when it is made amorphous by the ion implantation of germanium, there is little variation in a leak current characteristic, and, moreover, most of the

area of an impurity diffused layer 32 and the dependency of circumference length is not seen. Next, the result investigated about the cobalt thickness dependency of the leak current characteristic of the cobalt silicide layer 33 after 2nd RTA is shown in drawing 18 R> 8 and drawing 19 .

[0047] If the case where an ion implantation is carried out to the case where the ion implantation of the germanium is not carried out when the cobalt film is 10nm is compared from drawing 18 and 19, among them, a difference will hardly be seen about a leak current characteristic, but when the cobalt film is thickened with 18nm, it turns out that a clearly good leak current characteristic is acquired for the direction at the time of carrying out the ion implantation of the germanium.

[0048] In addition, although the sheet resistance of the cobalt silicide layer at the time of forming a cobalt silicide layer, having used thickness of the cobalt film as 18nm was investigated, they were about 4ohm/** irrespective of the existence of a germanium ion implantation. When the ion implantation of the germanium is carried out and it is made amorphous to a silicon substrate also by the above experimental result before forming the cobalt film, it turns out that few good junction properties of the area dependency of an impurity diffused layer, a circumference length dependency, and a cobalt thickness dependency are acquired.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view (the 1) showing the production process of the semiconductor device of 1 operation gestalt of this invention.
[Drawing 2] It is the sectional view (the 2) showing the production process of the semiconductor device of 1 operation gestalt of this invention.
[Drawing 3] It is the sectional view showing the experiment process which met the formation process of conventional cobalt silicide.
[Drawing 4] It is the sectional view showing an example of the spike generated by the formation process of conventional cobalt silicide.
[Drawing 5] It is the sectional view showing an experiment process when the amorphous layer at the time of forming cobalt silicide is too shallow.
[Drawing 6] It is the sectional view showing an experiment process when the amorphous layer at the time of forming cobalt silicide is too deep.
[Drawing 7] In 1 operation gestalt of this invention, it is the sectional view showing an experiment process when the amorphous layer at the time of forming cobalt silicide is the optimal.
[Drawing 8] It is the property Fig. showing the relation between the recrystallization rate of an amorphous layer, and temperature formed with 1 operation gestalt of this invention.
[Drawing 9] It is the sectional view showing the trial condition for investigating the magnitude of the leakage current of an impurity diffused layer.
[Drawing 10] It is a leak current characteristic Fig. by difference of the area of the cobalt silicide layer after removing unreacted cobalt after the 1st heat treatment formed by the conventional approach.
[Drawing 11] It is a leak current characteristic Fig. by difference of the circumference length of the cobalt silicide layer after removing unreacted cobalt after the 1st heat treatment formed by the conventional approach.
[Drawing 12] It is a leak current characteristic Fig. by difference of the area of the cobalt silicide layer after the 2nd heat treatment formed by the conventional approach.
[Drawing 13] It is a leak current characteristic Fig. by difference of the circumference length of the cobalt silicide layer after the 2nd heat treatment formed by the conventional approach.
[Drawing 14] In 1 operation gestalt of this invention, it is a leak current characteristic Fig. by difference of the area of the cobalt silicide layer after removing unreacted cobalt after the 1st heat treatment.
[Drawing 15] In 1 operation gestalt of this invention, it is a leak current characteristic Fig. by difference of the circumference length of the cobalt silicide layer after removing unreacted cobalt after the 1st heat treatment.
[Drawing 16] In 1 operation gestalt of this invention, it is a leak current characteristic Fig. by difference of the area of the cobalt silicide layer after the 2nd heat treatment.
[Drawing 17] In 1 operation gestalt of this invention, it is a leak current characteristic Fig. by difference of the circumference length of the cobalt silicide layer after the 2nd heat treatment.
[Drawing 18] It is the property Fig. (the 1) which investigated how the leakage current of a cobalt

silicide layer would change after the 2nd heat treatment with differences of the thickness of the cobalt film in a comparison in 1 operation gestalt of the conventional approach and this invention.

[Drawing 19] It is the property Fig. (the 2) which investigated how the leakage current of a cobalt silicide layer would change after the 2nd heat treatment with differences of the thickness of the cobalt film in a comparison in 1 operation gestalt of the conventional approach and this invention.

[Drawing 20] It is the sectional view showing the formation process of the cobalt silicide layer of the conventional approach.

[Description of Notations]

1 Silicon Substrate
2 LOCOS Oxide Film
3 Gate Oxide
4 Polysilicon KONN Film
5 Gate Electrode
6 Impurity Impregnation Layer
7 Sidewall
8 Impurity Impregnation Layer
9 Source Layer
10 Drain Layer
11 Amorphous Layer (Amorphous Layer)
12 Cobalt Film
13 Titanium Nitride Film
14 Cobalt Silicide Layer

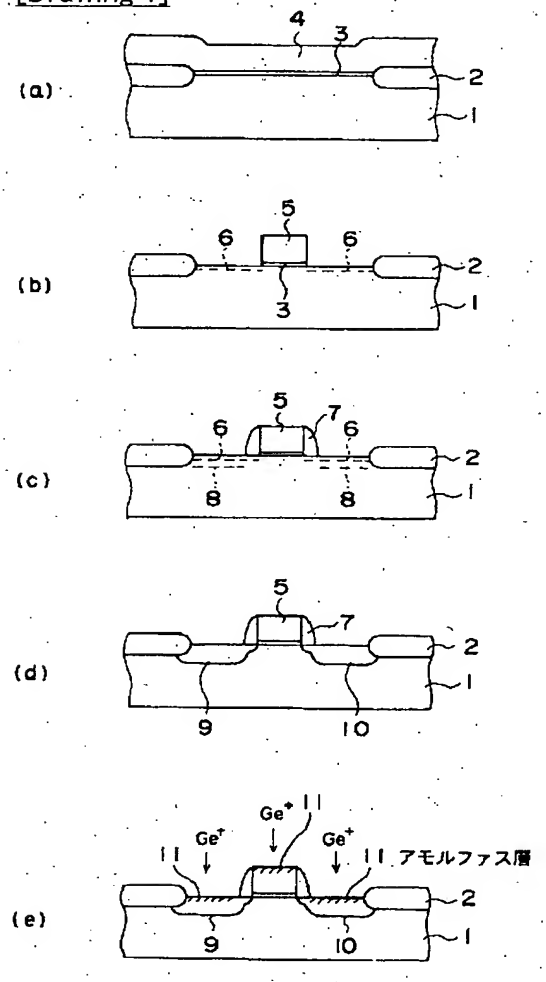
[Translation done.]

* NOTICES *

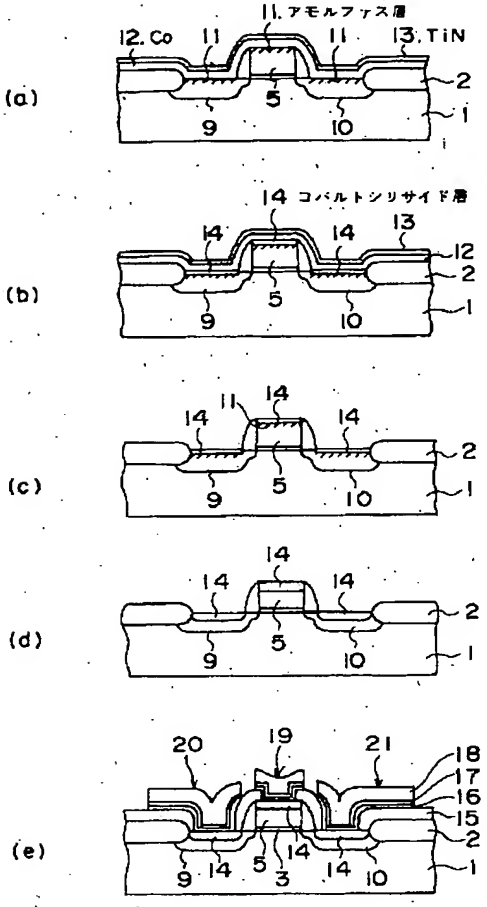
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

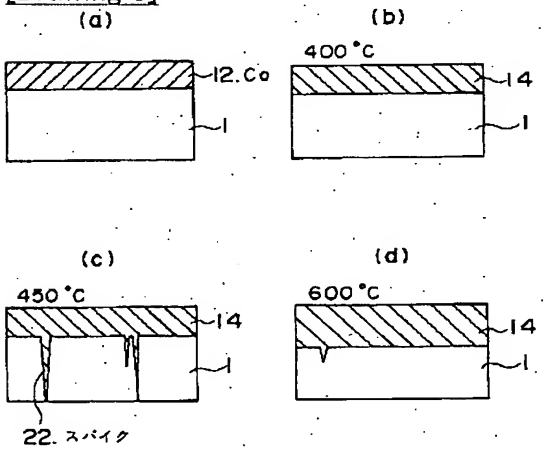
[Drawing 1]



[Drawing 2]



[Drawing 3]



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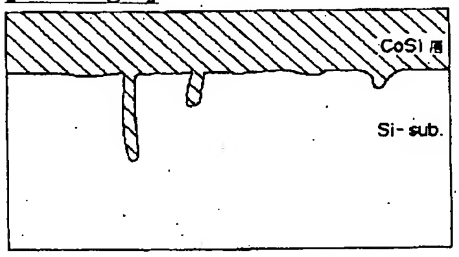
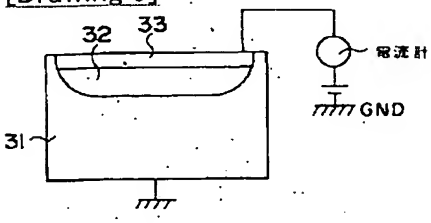


(1 st. F.A. 450°C. 30min ウオッシュアウト後)

[Drawing 9]



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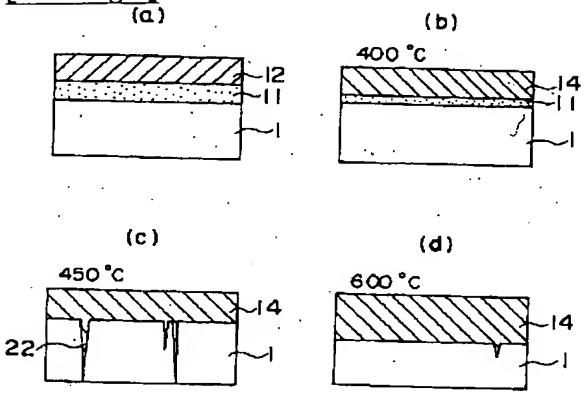
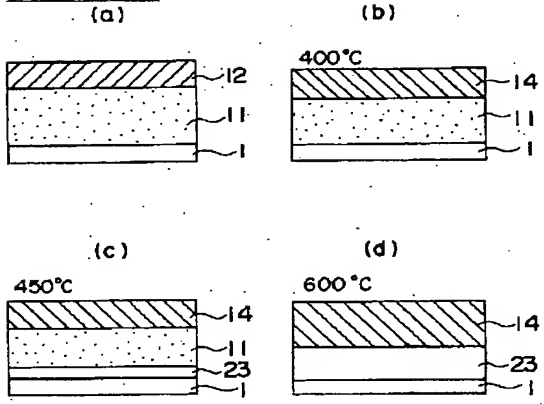


[Drawing 6]



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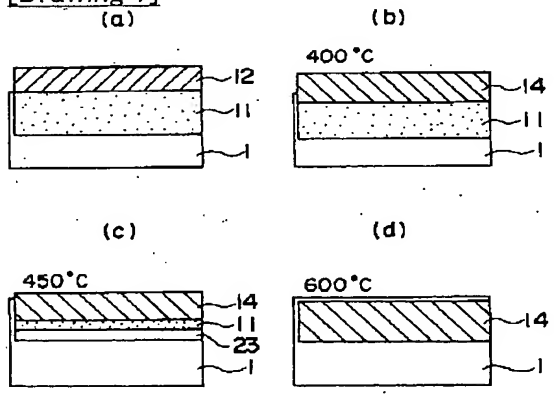
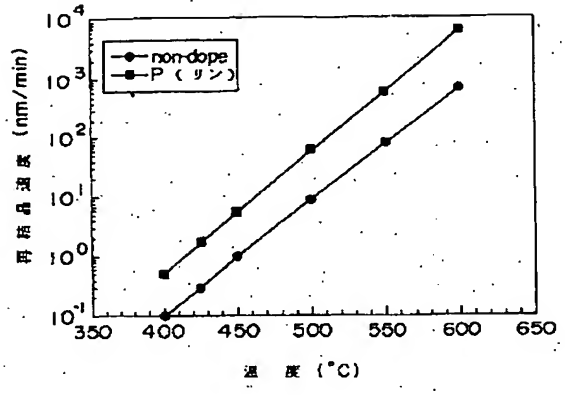
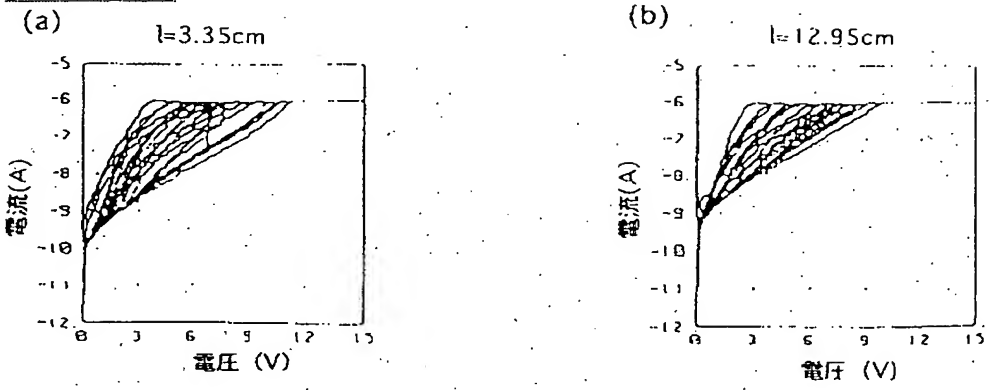


[Drawing 8]

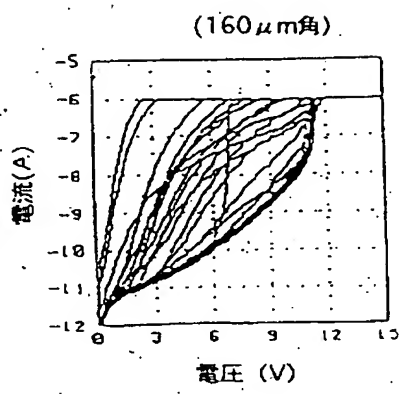


[Drawing 13]



[Drawing 10]

(a)



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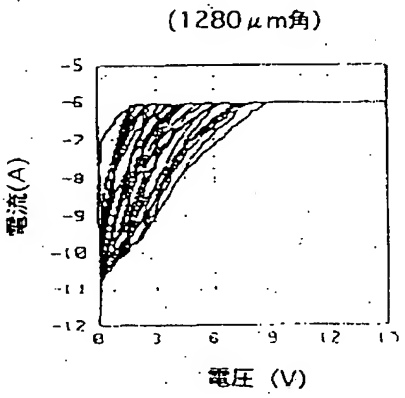

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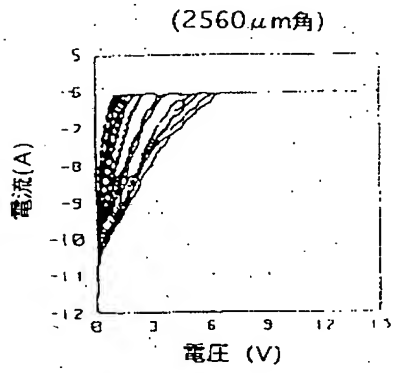

[Drawing 11]

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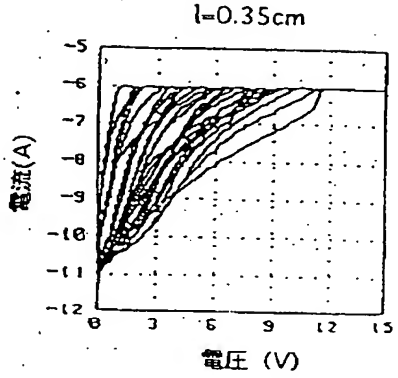

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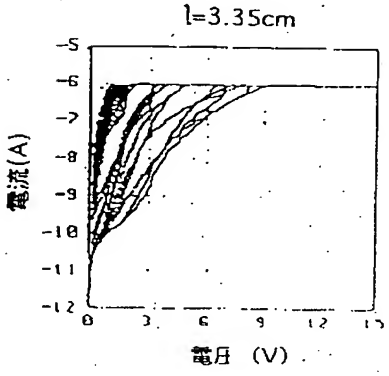

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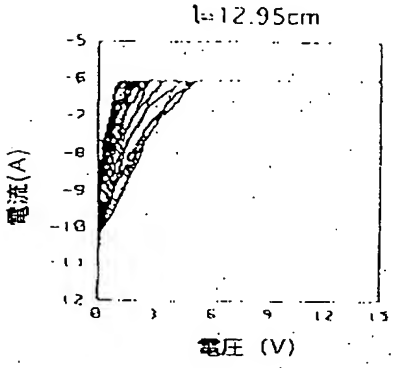
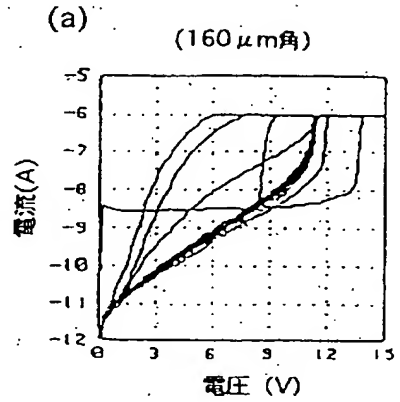
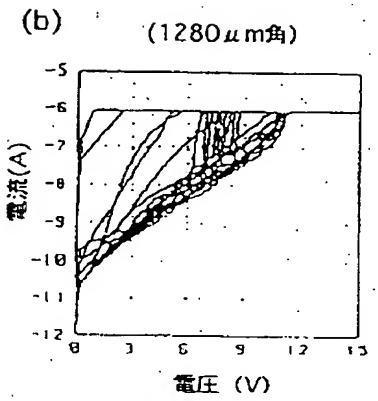
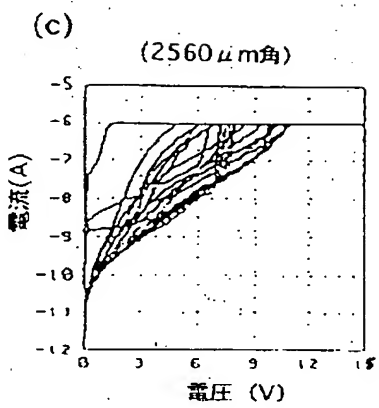


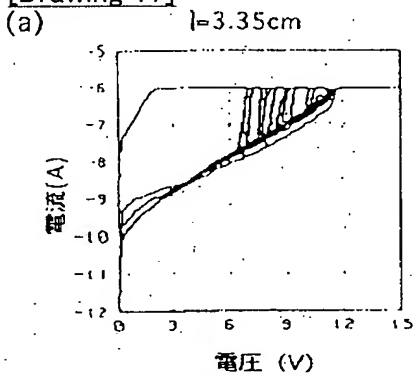
[Drawing 12]

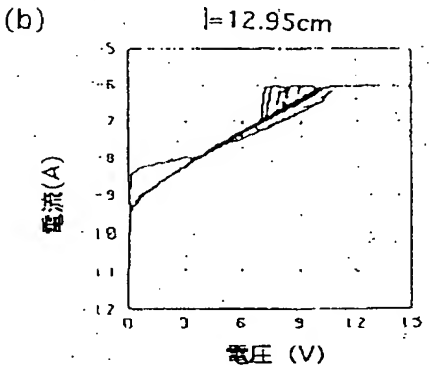






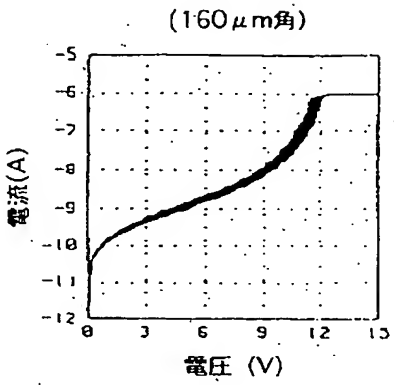
[Drawing 17]





[Drawing 14]

(a)



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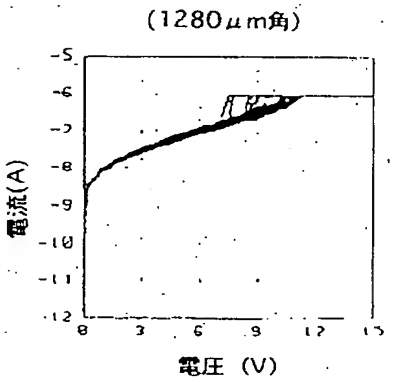

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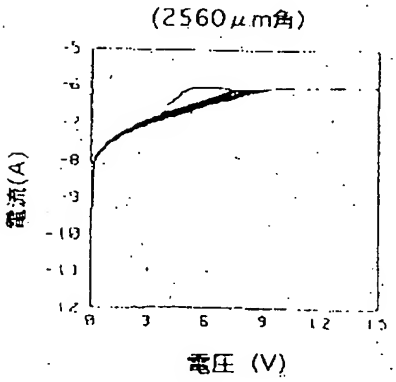
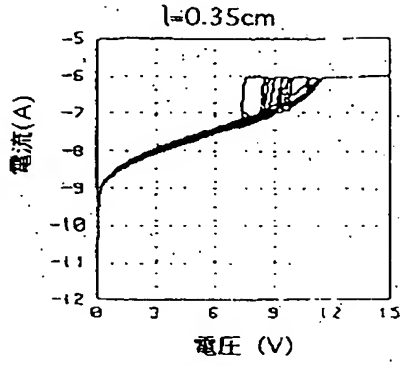


[Drawing 15]

(a)



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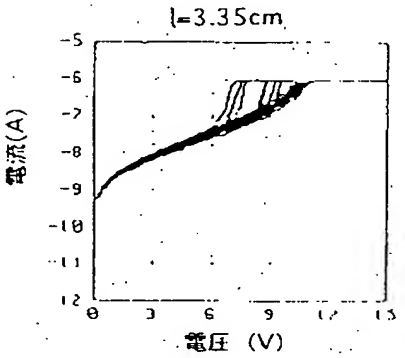

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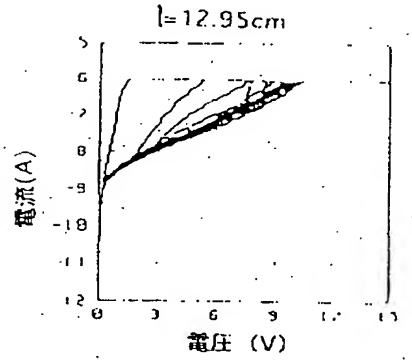
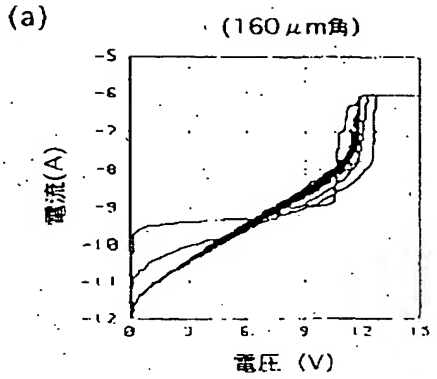
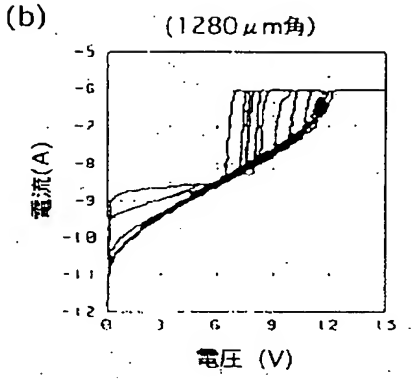
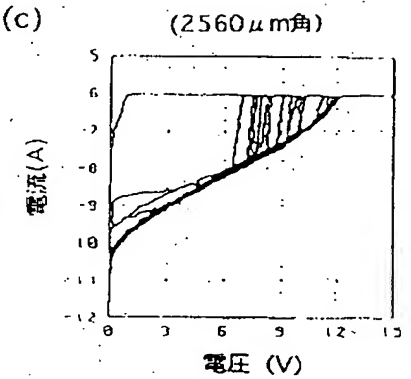


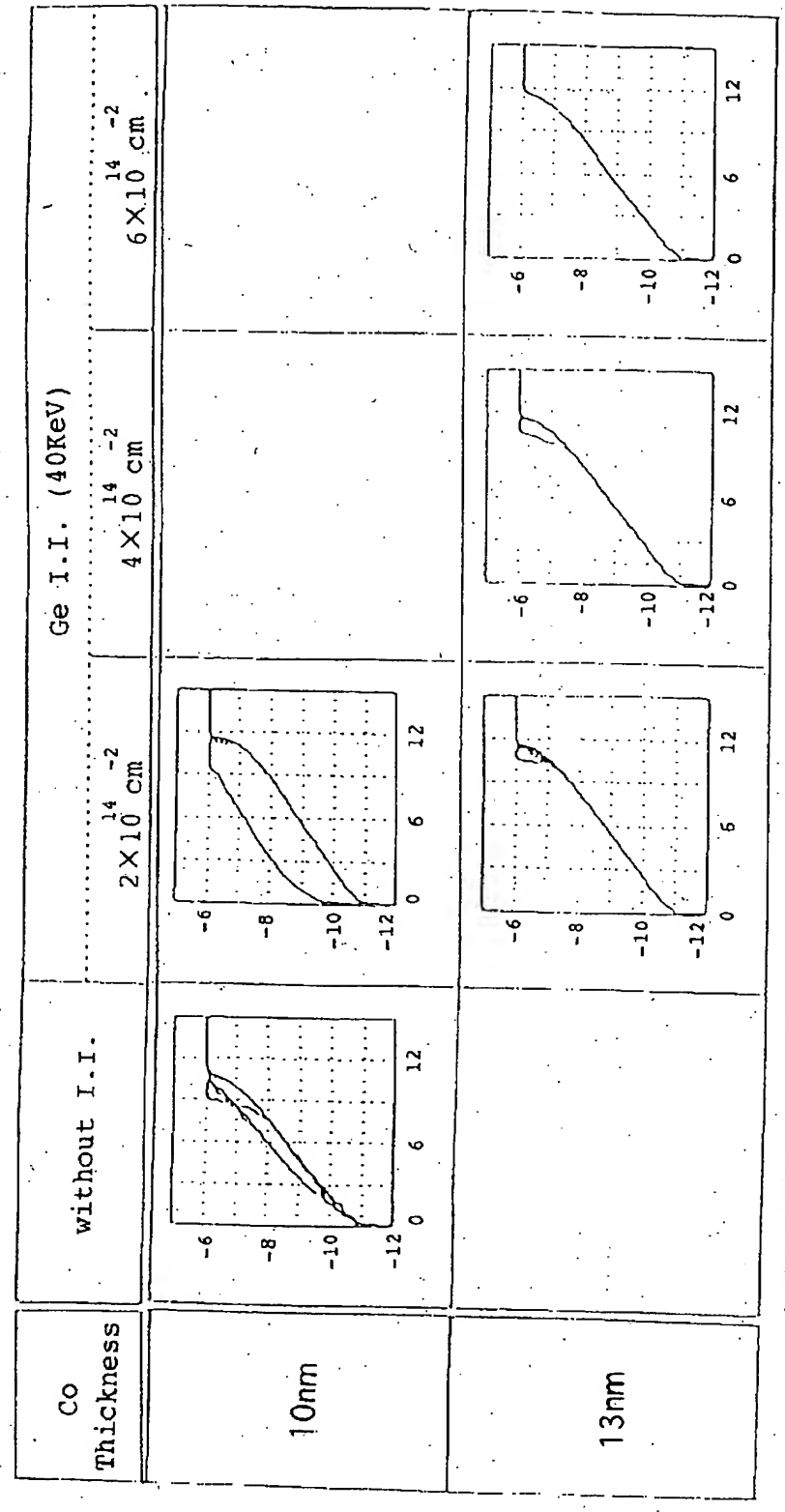
[Drawing 16]





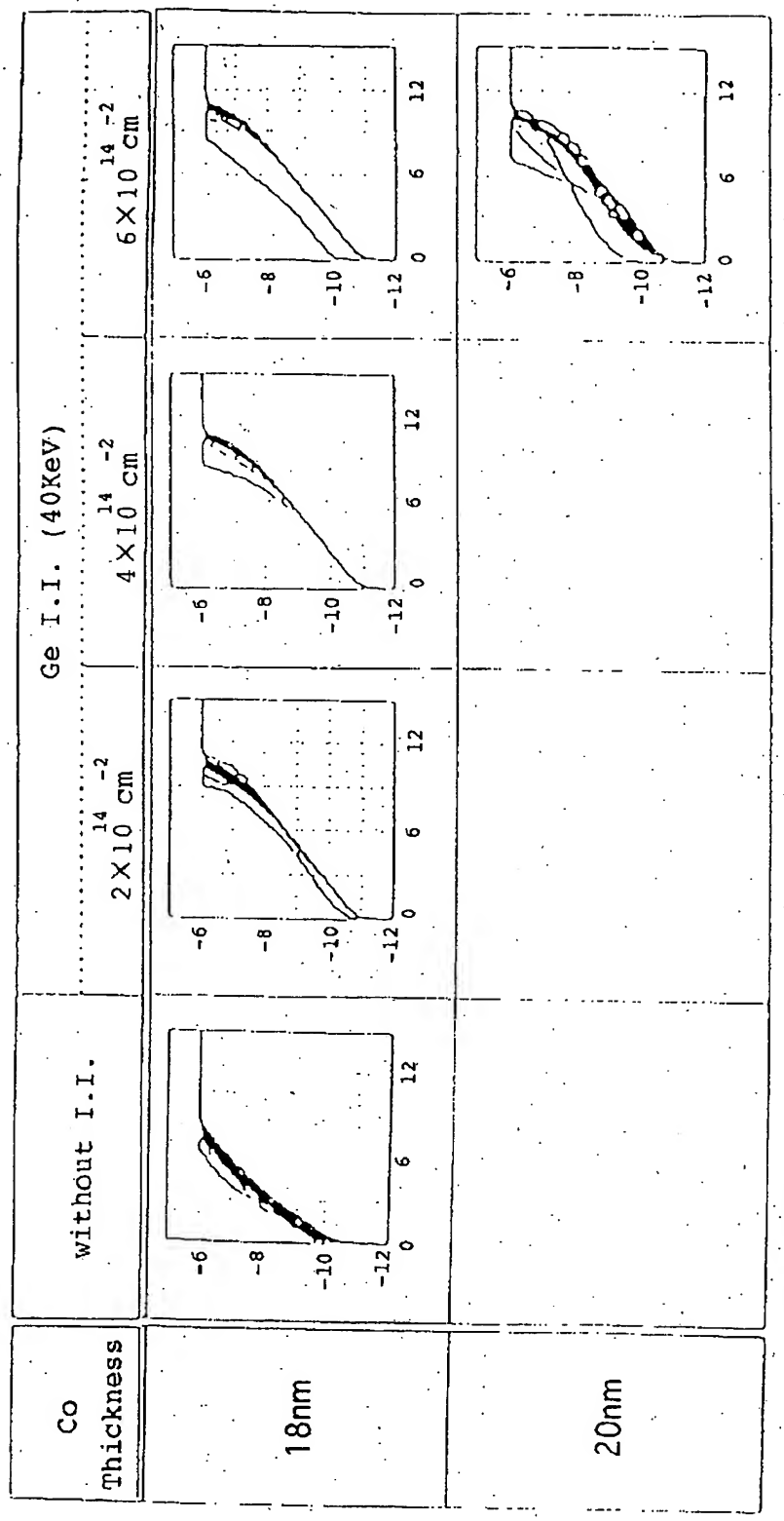


[Drawing 18]



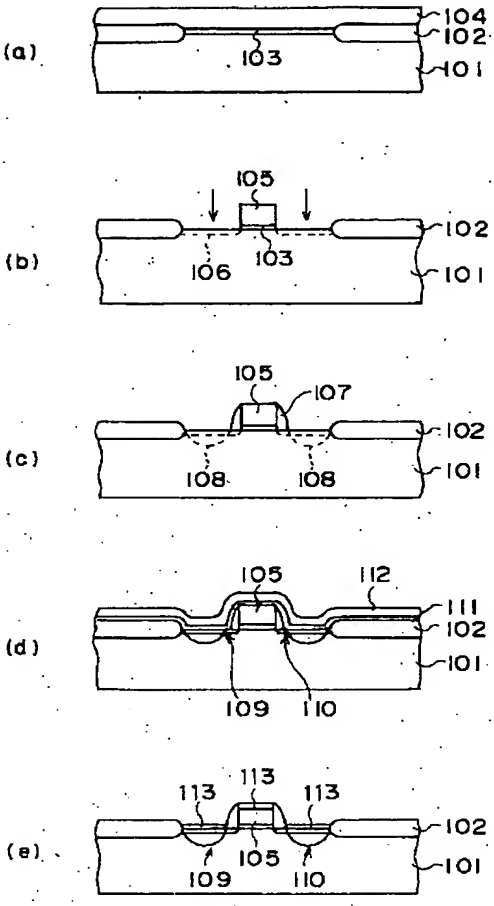
各横軸は電圧（V）を示す
各縦軸は電流（A）を示す

[Drawing 19]



各横軸は電圧（V）を示す
各縦軸は電流（A）を示す

[Drawing 20]



[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平9－251967

(43)公開日　平成９年(1997)９月22日

(51)Int.Cl.[6]		識別記号	庁内整理番号	Ｆ Ｉ		技術表示箇所
Ｈ０１Ｌ	21/28	３０１		Ｈ０１Ｌ	21/28	３０１Ｓ
	21/3205				21/88	Ｑ
	21/8238				27/08	３２１Ｆ
	27/092					

審査請求　未請求　請求項の数７　ＯＬ　（全 16 頁）

(21)出願番号　特願平8－58865

(22)出願日　平成８年(1996)３月15日

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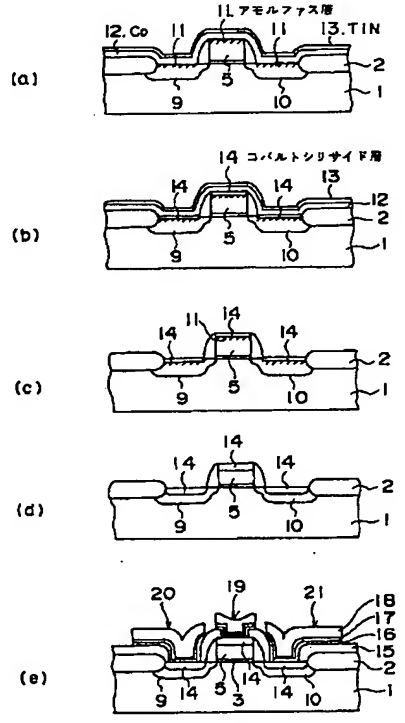
最終頁に続く

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】
【課題】サリサイドプロセスを有する半導体装置の製造方法に関し、底面でスパイクが生じ難いコバルトシリサイド層を形成すること。
【解決手段】シリコンよりなる不純物拡散層９の上層部にイオン注入により非晶質層１１を形成し、さらにコバルト膜１２を不純物拡散層９の上に形成した後に、１回目の熱処理によりコバルト膜１２と不純物拡散層９内のシリコンとを反応させてその非晶質層１１の上層部に低温でCoSi又はCo_2Si よりなるコバルトシリサイド層１４を形成し、続いて未反応のコバルトを除去し、ついで２回目の熱処理によってコバルトシリサイド層１４を構成するCoSi又はCo_2Si を$CoSi_2$ に変化させて低抵抗化するとともに、コバルトシリサイド層１４を初期の非晶質層１１の深さと同じかそれよりも深く入り込ませる工程を含む。



【特許請求の範囲】
【請求項１】シリコン層の上層部に不純物を導入し、熱処理により不純物拡散層を形成する工程と、
前記不純物拡散層の上層部に元素をイオン注入することにより非晶質層を形成する工程と、
前記非晶質層の上にコバルト膜を形成する工程と、
前記コバルト膜と前記不純物拡散層を第１の温度により加熱して、前記非晶質層の上層部にCo_2Si 又はCoSiよりなるコバルトシリサイド層を形成する工程と、
前記不純物拡散層内のシリコンと反応しなかった前記コバルト膜を除去する工程と、
前記コバルトシリサイド層及び前記不純物拡散層を第２の温度により加熱することにより、前記Co_2Si 又はCoSiを$CoSi_2$ に変化させるとともに、前記コバルトシリサイド層を前記非晶質層と同じ深さまたは前記非晶質層より深く形成する工程とを有することを特徴とする半導体装置の製造方法。
【請求項２】前記第１の温度は４５０℃以下であることを特徴とする請求項１記載の半導体装置の製造方法。
【請求項３】前記第２の温度は、５００℃以上であって不純物拡散層を形成する前記熱処理の際の温度よりも低いことを特徴とする請求項１記載の半導体装置の製造方法。
【請求項４】前記コバルト膜は８～２０nmの厚さに形成することを特徴とする請求項１記載の半導体装置の製造方法。
【請求項５】前記コバルト膜を形成後、前記熱処理を行う前に、前記コバルト膜上にキャップ層を形成することを特徴とする請求項１記載の半導体装置の製造方法。
【請求項６】前記元素は、ゲルマニウム、シリコン、砒素であることを特徴とする請求項１記載の半導体装置の製造方法。
【請求項７】前記ゲルマニウムは8×10^{13}atoms/cm^2 以上でイオン注入され、前記シリコンは8×10^{14} atoms/cm^2以上でイオン注入され、前記砒素は8×10^{13}atoms/cm^2 ～5×10^{14}atoms/cm^2 でイオン注入されることを特徴とする請求項６記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置の製造方法に関し、より詳しくは、サリサイドプロセスを有する半導体装置の製造方法に関する。
【０００２】
【従来の技術】今日の半導体デバイスの高集積化、高速度化のスピード化はめざましく、高速３次元画像処理や高速通信などを家庭のパソコンやゲーム機で簡単に楽しめるようになってきた。このような高性能化は、ＣＭＯＳデバイスのサイズを単に微細化することによって実現されてきた。現在のＣＭＯＳデバイスは、ゲート長が0.35μｍ程度の大きさの量産段階にあり、研究レベルでは0.1 ～0.05μｍのＣＭＯＳデバイスも報告されている。しかし、ゲート長が0.35μｍよりも小さくなるデバイスではスケーリング則に従わない寄生抵抗が大きくなり、従来のトレンド通りには性能が上がらない。そこでゲート、ソース及びドレインを同時にシリサイド化して低抵抗化するプロセス、即ちサリサイドプロセスが必須の技術になっている。
【０００３】ＭＯＳトランジスタにおいて、ショートチャネル効果などを抑えるために拡散層を浅くすると、拡散層の抵抗の増大をもたらすので、ゲート電極を構成するポリシリコン表面やソース層及びドレイン層の表面を自己整合的にシリサイド化して低抵抗化する技術が検討されている。そのシリサイドとしては、$TiSi_2$ 、$CoSi_2$ 、NiSiなどの材料が用いられる。
【０００４】次に、ゲート、ソース、ドレインの表層にCoサリサイドを用いたＭＯＳトランジスタの一般的な製造工程について説明する。まず、図２０(a) に示すように、シリコン基坂101 のうちLOCOS 酸化膜102 によって分離された領域の表面を熱酸化によって50Å程度のゲート酸化膜103 を形成する。続いて、その上にＣＶＤ法により1500Å程度の膜厚のポリシリコン膜104 を形成する。
【０００５】次に、図２０(b) に示すように、ポリシリコン膜104 内にボロン、リン或いは砒素のいずれかをイオン注入した後に、ポリシリコン膜104 をパターニングしてゲート電極105 を形成する。この後に例えば隣をイオン注入して浅い不純物注入層106 を形成する。次に、図２０(c) に示すようにＣＶＤ法により1000Å程度の厚さのシリコン酸化膜を形成し、ゲート電極105 が露出するまで異方性エッチングを行い、シリコン酸化膜をサイドウォール107 として残す。
【０００６】その後に、隣をイオン注入して深い不純物注入層108 を形成した後に、浅い不純物注入層106 と深い不純物注入層108 を加熱処理により活性化し、これによりゲート電極105 の両側のシリコン基板101 にＬＤＤ構造のソース層109 とドレイン層110 を形成することになる。次に、バッファードフッ酸によりゲート電極105 、ソース層109 、ドレイン層110 それぞれの表面のシリコン酸化膜（自然酸化膜）を除去した後に、図２０(d) に示すように 100Å程度のコバルト膜111 と 300Å程度の窒化チタン膜112 を形成し、550 ℃30秒のRTA(rapid thermal annealling) 処理によってシリサイド化してコバルトシリサイド層113 を形成する。
【０００７】続いて、図２０(e) に示すように窒化チタン膜112 と未反応のコバルト膜111とを除去し、さらに850 ℃30秒のRTA 処理を行い、これによりゲート電極105 、ソース層109 及びドレイン層110 の表面に形成されたコバルトシリサイド層114をさらに低抵抗化する。そのようなサリサイド技術は基本的な工程であり、その改良技術として、シリサイド層の平坦化技術が特開昭62-3

3466号公報に示され、また、シリサイド層の膜厚の均一化技術が特開平5-291180号公報に記載されている。

【０００８】

【発明が解決しようとする課題】以上のようなコバルトシリサイド層の形成は、ソース層及びドレイン層が深い場合には特に問題はないが、例えば１００nm程度まで浅くなってくると、リーク電流が流れやすくなるという問題がある。その原因としては、コバルトシリサイド層の底からコバルトシリサイドのスパイクが発生してソース層及びドレイン層を突き抜けるためと考えられる。このようなコバルトシリサイドのスパイクは、コバルトシリサイド層を上記した２つの特許公報に記載された方法や温度条件によって形成しても生じた。

【０００９】本発明は、このような問題に鑑みてなされたものであって、底面でスパイクが生じ難いコバルトシリサイド層を形成する工程を含む半導体装置の製造方法を提供することを目的とする。

【００１０】

【課題を解決するための手段】

（手段）上記した課題は、図１、２に例示するように、シリコン層１の上層部に不純物を導入し、熱処理により不純物拡散層９，１０を形成する工程と、前記不純物拡散層９，１０の上層部に元素をイオン注入することにより非晶質層１１を形成する工程と、前記非晶質層１１の上にコバルト膜１２を形成する工程と、前記コバルト膜１２と前記不純物拡散層９，１０を第１の温度により加熱して、前記非晶質層１１の上層部にCo_2 Si又はCoSiよりなるコバルトシリサイド層１４を形成する工程と、前記不純物拡散層９，１０内のシリコンと反応しなかった前記コバルト膜１２を除去する工程と、前記コバルトシリサイド層１４及び前記不純物拡散層９，１０を第２の温度により加熱することにより、前記Co_2Si 又はCoSiを$CoSi_2$ に変化させるとともに、前記コバルトシリサイド層１４を前記非晶質層１１と同じ深さ又は前記非晶質層１１より深く形成する工程とを有することを特徴とする半導体装置の製造方法によって解決する。

【００１１】上記半導体装置の製造方法において、前記第１の温度は４５０℃以下であることを特徴とする。上記半導体装置の製造方法において、前記第２の温度は、５００℃以上であって不純物拡散層を形成する前記熱処理の際の温度よりも低いことを特徴とする。上記半導体装置の製造方法において、前記コバルト膜は８～２０nmの厚さに形成することを特徴とする。

【００１２】上記半導体装置の製造方法において、前記コバルト膜を形成した後、前記熱処理を行う前に前記コバルト膜上に、コバルトと反応しないキャップ層（例えばTiN）を形成する工程を有することを特徴とする。上記半導体装置の製造方法において、前記元素は、ゲルマニウム、シリコン、砒素であることを特徴とする。この場合、前記ゲルマニウムは8×10^{13}atoms/cm^2 以上でイオン注入され、前記シリコンは8×10^{14} atoms/cm^2 以上でイオン注入され、前記砒素は8×10^{13}atoms/cm^2 ～5×10^{14}atoms/cm^2 でイオン注入されることを特徴とする。

【００１３】（作用）次に、本発明の作用について説明する。本発明によれば、不純物拡散層の上層部にコバルトシリサイド層を形成するために、シリコンよりなる不純物拡散層の上層部にイオン注入により非晶質層を形成し、さらにコバルト膜を不純物拡散層の上に形成した後に、１回目の熱処理によりコバルト膜と不純物拡散層内のシリコンとを反応させてその非晶質層の上層部に低温でCoSi又はCo_2Si よりなるコバルトシリサイド層を形成し、続いて未反応のコバルト膜を除去し、ついで２回目の熱処理によってコバルトシリサイド層を構成するCoSi又はCo_2Si を$CoSi_2$ に変化させてシート抵抗を低抵抗化するとともに、コバルトシリサイド層を初期の非晶質層の深さと同じかそれよりも深く入り込ませている。

【００１４】このような工程によれば、コバルトシリサイド層を形成するための１回目の熱処理及び２回目の熱処理の際に、コバルトシリサイド層の構成元素の下方への移動が非晶質層によって妨げられ、コバルトシリサイド層のスパイクの発生は防止される。しかも、２回目の熱処理の際に、非晶質層の初期の深さまでコバルトシリサイド層を広げて、非晶質層が再結晶化してもその再結晶がコバルトシリサイド層により浸漬させるようにしたので、抵抗の高い再結晶とコバルトシリサイド層との接合が妨げられ、コンタクト抵抗の上昇が防止される。

【００１５】その１回目の熱処理の温度が４５０℃以上になると、非晶質層が下から再結晶化してしまうので、非晶質化した意味がなくなる。また、２回目の熱処理の温度が不純物拡散層を活性化するための温度以上であれば、シリサイド層からコバルトが溶け出して接合リークを増大させるので好ましくない。このようなコバルトシリサイド層はＭＯＳトランジスタのソース層、ドレイン層などに使用されてそれらの層を低抵抗化する。

【００１６】なお、非晶質層を形成するためにイオン注入する元素は、特に限定するものではないが、質量の大きなゲルマニウム、シリコンや、ドーパントに使用される砒素などが好ましい。

【００１７】

【発明の実施の形態】そこで、以下に本発明の実施形態を図面に基づいて説明する。以下に、本発明の実施の形態について説明する。図１は、本発明の一実施形態の工程を示す断面図である。まず、図１(a) に示すように、シリコン基坂１のうちLOCOS 酸化膜２によって分離された領域の表面を熱酸化し、これによって厚さ5nm 程度のゲート酸化膜３を形成する。続いて、ゲート酸化膜３及びLOCOS 酸化膜２の上にＣＶＤ法により150nm 程度の膜厚のポリシリコン膜４を形成する。

【００１８】次に、図１(b) に示すように、ポリシリコ

ン膜４内に例えば砒素をイオン注入した後に、ポリシリコン膜４及びゲート酸化膜３をパターニングしてポリシリコン膜４によりゲート電極５を形成する。この後に、ゲート電極５をマスクに使用して例えば砒素をシリコン基板１にイオン注入して浅い不純物注入層６を形成する。そのイオン注入のドーズ量は3×10^{14}atm/cm^2 であり、その加速エネルギーは１０keV である。

【００１９】次に、ＣＶＤ法により100nm 程度の厚さのシリコン酸化膜を形成する。続いて、ゲート電極５の上面が露出するまでシリコン酸化膜を垂直方向に異方性エッチングして、図１(c) に示すようにシリコン酸化膜をゲート電極５の側面にサイドウォール７として残す。その後に、ゲート電極５をマスクに使用して砒素をシリコン基板１にイオン注入して深い不純物注入層８を形成する。そのイオン注入のドーズ量は2×10^{15}atm/cm^2 であり、その加速エネルギーは４０keV である。

【００２０】次に、１０００℃で１０秒間のＲＴＡ処理によってゲート電極５内の砒素を内部に拡散させるとともに、浅い不純物注入層６と深い不純物注入層８の砒素を活性化させて図１(d) に示すようなＬＤＤ構造のソース層９とドレイン層１０をゲート電極５の両側のシリコン基板１に形成する。この場合、ソース層９とドレイン層１０のうちサイドウォール７に重ならない領域の深さはシリコン基板１の表面から１００nm程度となる。

【００２１】その後に、図１(e) に示すように、ソース層９、ドレイン層１０を含む全体にゲルマニウムをイオン注入し、これによりゲート電極５、ソース層９及びドレイン層１０の表層にアモルファス（非晶質）層１１を形成する。そのイオン注入は、ドーズ量8×10^{13}atm/cm^2 以上である。また、イオン注入時の加速エネルギーは、ソース層９とドレイン層１０の底よりも浅くアモルファス層１１が形成され、しかも後のシリサイド化用第１回目加熱処理時にアモルファス層１１が消失しない程度に深く、さらにシリサイド化用第２回目加熱処理時にアモルファス層１１が消失する大きさに設定する。

【００２２】具体的には、これから形成しようとするシリサイド層の深さによるが、ソース層９、ドレイン層１０の深さが１００nmの場合に、２０～４０keV 程度の範囲内にある。続いて、バッファードフッ酸によりゲート電極５、ソース層９、ドレイン層１０それぞれの表面のシリコン酸化膜を除去する。バッファードフッ酸は、フッ酸を２、水を１００の割合の混合液であり、その除去時間は６０秒程度である。

【００２３】次に、図２(a) に示すように全体に厚さ８～２０nm程度のコバルト（Co）膜１２と３０nm程度の窒化チタン（TiN ）膜１３をスパッタにより順次形成する。コバルト膜１２の成長の際には、成長雰囲気圧力を５mTorr 、成長雰囲気へのアルゴンガス流量を１００sccm、コバルトターゲットに印加する直流電力量を0.2W/cm^{2}とした。コバルト膜１２の厚さは、ゲルマニウムイオン注入エネルギーを大きくするほど厚くする。

【００２４】また、窒化チタン膜１３の成長の際には、成長雰囲気圧力を５mTorr 、成長雰囲気へのアルゴンガス流量を５０sccm、窒素ガス流量を５０sccm、窒化チタンターゲットに印加する直流電力量を7.0W/cm^{2}とした。窒化チタン膜１３は、シリサイド化の際にシリサイド層の表面に凹凸が生じるのを抑制するために形成される。

【００２５】その後に、上記したシリサイド化用第１回目加熱処理を行う。即ち、図２(b)に示すように、窒素又はアルゴンの雰囲気中で、４００～４５０℃で３０秒間のＲＴＡ(rapid thermal annealling)処理を行ってゲート電極５、ソース層９、ドレイン層１０のそれぞれの表面をシリサイド化すると、アモルファス層１１の上部にCo_2Si 又はCoSiよりなるコバルトシリサイド層１４が形成される。なお、ＲＴＡ温度が４００℃よりも低くなると、コバルトシリサイド層１４は形成されず、また、４５０℃よりも高くなるとアモルファス層１１の下が再結晶化されるので好ましくない。この加熱処理時には、アモルファス層１１の上部がコバルトシリサイド層１４によって浸食されるだけでなく、アモルファス層１１のうち底から単結晶化してくるが、上記したようにゲルマニウムのイオン注入エネルギーを最適化しているので、この段階でアモルファス層１１が消滅することはなく、わずかでも残っている。

【００２６】次に、図２(c) に示すように、７０℃に加熱した過酸化水素とアンモニア水の混合液(H_2O_2:NH_4OH:H_2O ＝１：１：４）に１８０秒間浸けることにより窒化チタン膜１３を除去し、続けて硫酸と過酸化水素の混合液(H_2SO_4:H_2O_2 ＝３：１）に２０分間浸けることにより未反応のコバルト膜１２を除去する。この場合、コバルトシリサイド層１４はそのまま残る。

【００２７】次に、シリサイド化用第２回目加熱処理を行う。即ち、図２(d) に示すように、窒素又はアルゴンの雰囲気中でコバルトシリサイド層１４を６００℃～９００℃の温度範囲で加熱する。これにより、コバルトシリサイド層１４はCo_2Si 又はCoSiから$CoSi_2$ に変わって低抵抗化する。この場合、６００℃よりも加熱温度を低くすると、$CoSi_2$ が生じにくくなって低抵抗化が達成できなくなる。また、９００℃以上よりも加熱温度が高くなると、コバルトシリサイド層１４からCo原子が溶け出し接合リークを増大させる。

【００２８】これにより得られたコバルトシリサイド層１４の厚さは、ソース層９及びドレイン層１０を構成する不純物拡散層の残った厚さを１とすると、0.5 ～2.0 程度になる。この後に、図２(e) に示すように、全体にＣＶＤ法により７００nmの厚さのシリコン酸化膜１５を形成し、ついで、シリコン酸化膜１５をパターニングしてゲート電極５、ソース層９及びドレイン層１０の上にコンタクトホールを形成した後に、膜厚２０nmのチタン膜１６、膜厚１００nmの窒化チタン膜１７、膜厚５００

nmのアルミ層１８を形成し、これらの３つの層１６～１８をフォトリソグラフィー法によってパターニングして一般的なゲート引出電極１９、ソース引出電極２０、ドレイン引出電極２１を形成する。

【００２９】なお、上記した説明では、アモルファス層１４を形成するためにゲルマニウムを使用したが、シリコン、砒素、硼素など他の元素をイオン注入しても良い。なお、元素の質量や、不純物拡散層の不純物濃度の制御などを考慮すると、ゲルマニウム、シリコンが好ましい。ゲルマニウムは8×10^{13} atoms/cm^{2}以上でイオン注入され、シリコンは8×10^{14} atoms/cm^{2}以上でイオン注入され、砒素は8×10^{13}atoms/cm^2 ～5×10^{14} atoms/cm^{2}でイオン注入される。

【００３０】以上のような工程により形成されたＭＯＳトランジスタにおけるコバルトシリサイド層１４の底部には殆どスパイクが発生せず、リーク電流が抑制された。以下に、コバルトシリサイド層１４のスパイク発生について詳述する。図３(a) に示すように、シリコン基板１をアモルファス化しないでその上に膜厚１０nmのコバルト層１２を形成した後に次に示すような第１の実験を行った。

【００３１】まず、図３(b) に示すように、コバルト層１２及びシリコン基板１を４００℃で加熱したところ、Co_2Si で示されるコバルトシリサイド層１４がシリコン基板１の表層に形成された。次に、図３(c) に示すように、コバルトシリサイド層１４及びシリコン基板１を４５０℃で加熱したところ、コバルトシリサイド層１４を構成していたCo_2Si がCoSiに変化した。続いて、図３(d) に示すように、コバルトシリサイド層１４をさらに６００℃で加熱したところ、CoSiが$CoSi_2$ に変化し、しかもコバルトシリサイド層１４の底面にはスパイク２２が生じていた。未反応コバルトを除去した後の$CoSi_2$ とSiの界面の断面図をＴＥＭ観察したところ、図４に示すようになり、その界面は凹凸があり、最大で約８０nmのつらら状の異常成長（スパイク）が生じていた。

【００３２】次に、図５(a) に示すように、シリコン基板１を表面から浅くアモルファス化した後に、その上に膜厚１０nmのコバルト層１２を形成し、ついで次に示すような第２の実験を行った。まず、図５(b) に示すように、コバルト層１２及びシリコン基板１を４００℃で加熱したところ、Co_2Si で示されるコバルトシリサイド層１４がシリコン基板１表層に形成され、その底部には薄いアモルファス層１１が残った。つぎに、図５(c) に示すように、４００℃で加熱されたコバルト層１４及びシリコン基板１をさらに４５０℃で加熱したところ、コバルトシリサイド層１４を構成するCo_2Si がCoSiに変わり、しかもコバルトシリサイド層１４がアモルファス層１１を全て浸食した。そしてコバルトシリサイド層１４の底面にはスパイクが生じていた。さらに、図５(d) に示すように、コバルトシリサイド層１４を再び６００℃で加熱したところ、$CoSi_2$ で示されるコバルトシリサイド層１４が形成され、その底面にはスパイク２２が生じていた。

【００３３】次に、図６(a) に示すように、シリコン基板１の表層を深くアモルファス化した後に膜厚１０nmのコバルト層１２を生成し、さらに次に示す第３の実験を行った。まず、図６(b) に示すように、コバルト層１２及びシリコン基板１を４００℃で加熱したところ、Co_2Si で示されるコバルトシリサイド層１４がシリコン基板１の表層に形成され、その底部には厚いアモルファス層１１が残った。続いて、図６(c) に示すように、４００℃で加熱されたコバルトシリサイド層１４及びシリコン基板１をさらに４５０℃で加熱したところ、コバルトシリサイド層１４を構成するCo_2Si がCoSiに変わり、その下方にはアモルファス層１１が存在したが、アモルファス層１１の底部はわずかに再結晶化していた。さらに、図６(d) に示すように、コバルトシリサイド層１４を再び６００℃で加熱したところ、$CoSi_2$ で示されるコバルトシリサイド層１４が形成され、その底面にはスパイク２２が生ぜず、しかも、その下方ではアモルファス層１１が再結晶化した結果のシリコン層２３が存在していた。

【００３４】従って、コバルトシリサイド層１４からのスパイクの発生を防止するためには第３の実験の工程のようにアモルファス層１１を十分に深くすればよいとも考えられる。しかし、再結晶化したシリコン層２３には実際には図２に示すようにソース層及びドレイン層が存在し、アモルファス層１１内の不純物の活性化は８５０℃程度の加熱温度では十分ではなく、コバルトシリサイド層１４とソース層／ドレイン層とのコンタクト抵抗が十分に低減できなくなる。これにより、ソース層及びドレイン層の低抵抗化というシリサイド化の当初の目的を達成できない。

【００３５】次に、図７(a) に示すように、シリコン基板の表層をアモルファス化した後に膜厚１０nmのコバルト層１２を形成し、さらに、次に示す第４の実験を行った。この実験では、アモルファス層１１の深さを適正な値にした、即ち、１回目の加熱処理後にコバルトシリサイド層１４の下にアモルファス層１１が存在し、また、６００℃の再加熱処理ではアモルファス層１１のうちの再結晶化したシリコン層２３もコバルトシリサイド層１４によって浸食されるようにした。

【００３６】まず、図７(b) に示すように、コバルト層１２及びシリコン基板１を４００℃で３０秒間加熱したところ、Co_2Si で示されるコバルトシリサイド層１４がシリコン基板１表層に形成され、その下方にはアモルファス層１１が残った。続いて、図７(c) に示すように、コバルトシリサイド層１４及びシリコン基板１をさらに４５０℃で３０秒間加熱したところ、コバルトシリサイド層１４を構成するCo_2Si がCoSiに変わった。また、そ

のコバルトシリサイド層１４は、厚さが２０．２nmであり、そのうち２．０nmがシリコン基板１の表面から突出した状態となった。また、コバルトシリサイド層１４の下方には再結晶したシリコン層２３とアモルファス層１１が存在し、これらの厚さは合計で１８．２nm以下であった。

【００３７】さらに、図7(d) に示すように、コバルトシリサイド層１４及びシリコン基板１を６００℃で３０秒間、再加熱したところ、コバルトシリサイド層１４を構成していたCoSiが$CoSi_2$ となり、厚さが３５．２nmと厚くなった。この場合、コバルトシリサイド層１４はシリコン基板１の表面から１．２nm沈んで存在したので、当初のアモルファス層１４は完全にコバルトシリサイド層１４に浸食され、しかもその下方には再結晶化したシリコン層２３は存在しなかった。

【００３８】従って、コバルトシリサイド層１４の下に存在するソース層とドレイン層は最初に１０００℃程度で活性化された低抵抗の状態を維持したままであり、これによりコバルトシリサイド層１４とソース層、ドレイン層とのコンタクト抵抗は良好であった。また、$CoSi_2$ とSiの界面をＴＥＭ観察したところ図４のような異常成長はみられず、その界面は比較的平坦であった。

【００３９】以上のことから、膜厚１０nm～２０nmのコバルト膜を形成し、これを第１回目で４００℃～４５０℃の温度、第２回目で６００～９００℃の温度でそれぞれ３０秒間加熱して$CoSi_2$ のコバルトシリサイド層１４を形成する場合には、それぞれの膜厚に対して約１８．２nm～２６．４nm以上３５．２nm～７０．２nm以下の深さになるようにアモルファス層１１を形成する必要があることがわかった。

【００４０】また、Co_2Si 又はCoSiよりなるシリサイド層１４を形成する場合には、シリサイド反応が起こりかつアモルファス層１１の再結晶速度を極端に遅くする温度条件で行うと効果的である。例えば、図８に示すように４５０℃以下でアモルファス層１１の再結晶速度が極端に遅くなる。また、アモルファス層１１を形成する場合に、不純物を含有しない場合よりも不純物を含有する場合の方が再結晶速度が遅いことがわかる。

【００４１】最後に、コバルトシリサイド層のリーク電流について説明する。リーク電流は図９に示すように、シリコン基板３１を接地する一方、不純物拡散層３２の上層部のコバルトシリサイド層３３に正の電圧を印加した。まず、ゲルマニウムをイオン注入しない場合について説明する。５５０℃、３０秒間の第１回目のＲＴＡによってコバルトシリサイド層３３を形成してその後に未反応のコバルトを除去した直後、即ちウォッシュアウト直後の、リーク電流とバイアス電圧の関係（以下、リーク電流特性という）について不純物拡散層３２の平面積を変えて調査したところ、図１０(a) ～(c) に示すような結果が得られ、また、リーク電流特性について不純物拡散層３２の周辺長を変えて調査したところ、図１１(a) ～(c) に示すような結果が得られた。

【００４２】さらに、８２５℃、３０秒間の第２回目のＲＴＡによって$CoSi_2$ よりなるコバルトシリサイド層３３を形成した後のリーク電流特性について不純物拡散層３２の面積を変えて調査したところ、図１２(a) ～(c) に示すような結果が得られ、また、リーク電流特性について不純物拡散層３２の周辺長を変えて調査したところ、図１３(a),(b) に示すような結果が得られた。

【００４３】図１０～図１３によれば、１回目のＲＴＡの後のリーク電流特性は２回目のＲＴＡのリーク電流特性よりも悪く、また、不純物拡散層３２の面積が大きく又は周辺長が長くなる程劣化している。これは、コバルトシリサイド層３３の底部のスパイクによるものである。次に、ゲルマニウムを注入して不純物拡散層３２の上層部を予めアモルファス化した場合を説明する。

【００４４】５５０℃、３０秒間の第１回目のＲＴＡを経てウォッシュアウト直後のリーク電流特性について不純物拡散層３２の平面積を変えて調査したところ、図１４(a) ～(c) に示すような結果が得られ、また、リーク電流特性について不純物拡散層３２の周辺長を変えて調査したところ、図１５(a) ～(c) に示すような結果が得られた。

【００４５】さらに、８２５℃、３０秒間の第２回目のＲＴＡによって$CoSi_2$ よりなるコバルトシリサイド層３３を形成した後のリーク電流特性について不純物拡散層３２の面積を変えて調査したところ、図１６(a) ～(c) に示すような結果が得られ、また、リーク電流特性について不純物拡散層３２の周辺長を変えて調査したところ、図１７(a),(b) に示すような結果が得られた。

【００４６】図１４～図１７によれば、ゲルマニウムのイオン注入によりアモルファス化した場合には、リーク電流特性のバラツキは少なく、しかも不純物拡散層３２の面積、周辺長の依存性は殆ど見られない。次に、２回目のＲＴＡの後のコバルトシリサイド層３３のリーク電流特性のコバルト膜厚依存性について調べた結果を図１８及び図１９に示す。

【００４７】図１８、１９から、コバルト膜が１０nmの場合において、ゲルマニュウムをイオン注入しない場合とイオン注入した場合とを比べると、それらの間にはリーク電流特性については殆ど差異は見られないが、コバルト膜を１８nmと厚くした場合にゲルマニュウムをイオン注入した場合の方が明らかに良好なリーク電流特性が得られることがわかる。

【００４８】なお、コバルト膜の厚さを１８nmとしてコバルトシリサイド層を形成した場合のコバルトシリサイド層のシート抵抗を調べたが、ゲルマニウムイオン注入の有無にかかわらず、約４Ω／□であった。以上の実験結果によっても、コバルト膜を形成する前にシリコン基板にゲルマニウムをイオン注入してアモルファス化する

と、不純物拡散層の面積依存性、周辺長依存性、コバルト膜厚依存性の少ない良好な接合特性が得られることがわかる。

【００４９】

【発明の効果】以上述べたように本発明によれば、不純物拡散層の上層部にコバルトシリサイド層を形成するために、シリコンよりなる不純物拡散層の上層部にイオン注入により非晶質層を形成した後に、コバルト膜を不純物拡散層の上に形成した後に、１回目の熱処理によりコバルト膜と不純物拡散層内のシリコンとを反応させてその非晶質層の上層部に低温でCoSi又はCo_2Si よりなるコバルトシリサイド層を形成し、続いて未反応のコバルト膜を除去し、ついで２回目の熱処理によってコバルトシリサイド層を構成するCoSi又はCo_2Si を$CoSi_2$ に変化させて低抵抗化するとともに、コバルトシリサイド層を初期の非晶質層と同じかそれよりも深く入り込ませているたので、コバルトシリサイド層を形成するための１回目の熱処理及び２回目の熱処理の際に、コバルトシリサイド層の構成元素の下方への移動が非晶質層によって妨げられ、コバルトシリサイド層のスパイクの発生を防止することができる。しかも、２回目の熱処理の際に、非晶質層の初期の深さまでコバルトシリサイド層を広げるようにし、非晶質層が再結晶化してもその再結晶がコバルトシリサイド層により浸漬されるので、抵抗の高い再結晶とコバルトシリサイド層との接合が妨げられ、コンタクト抵抗が上昇することを防止できる。

【図面の簡単な説明】

【図１】本発明の一実施形態の半導体装置の製造工程を示す断面図（その１）である。

【図２】本発明の一実施形態の半導体装置の製造工程を示す断面図（その２）である。

【図３】従来のコバルトシリサイドの形成工程に沿った実験過程を示す断面図である。

【図４】従来のコバルトシリサイドの形成工程によって生成されたスパイクの一例を示す断面図である。

【図５】コバルトシリサイドを形成する際のアモルファス層が浅すぎる場合の実験過程を示す断面図である。

【図６】コバルトシリサイドを形成する際のアモルファス層が深すぎる場合の実験過程を示す断面図である。

【図７】本発明の一実施形態において、コバルトシリサイドを形成する際のアモルファス層が最適な場合の実験過程を示す断面図である。

【図８】本発明の一実施形態で形成されるアモルファス層の再結晶速度と温度の関係を示す特性図である。

【図９】不純物拡散層のリーク電流の大きさを調べるための試験状態を示す断面図である。

【図１０】従来方法により形成された１回目熱処理後に未反応コバルトを除去した後のコバルトシリサイド層の面積の相違によるリーク電流特性図である。

【図１１】従来方法により形成された１回目熱処理後に未反応コバルトを除去した後のコバルトシリサイド層の周辺長の相違によるリーク電流特性図である。

【図１２】従来方法により形成された２回目熱処理後のコバルトシリサイド層の面積の相違によるリーク電流特性図である。

【図１３】従来方法により形成された２回目熱処理後のコバルトシリサイド層の周辺長の相違によるリーク電流特性図である。

【図１４】本発明の一実施形態において、１回目熱処理後に未反応コバルトを除去した後のコバルトシリサイド層の面積の相違によるリーク電流特性図である。

【図１５】本発明の一実施形態において、１回目熱処理後に未反応コバルトを除去した後のコバルトシリサイド層の周辺長の相違によるリーク電流特性図である。

【図１６】本発明の一実施形態において、２回目熱処理後のコバルトシリサイド層の面積の相違によるリーク電流特性図である。

【図１７】本発明の一実施形態において、２回目熱処理後のコバルトシリサイド層の周辺長の相違によるリーク電流特性図である。

【図１８】従来方法と本発明の一実施形態に比較において、コバルト膜の膜厚の相違によって２回目熱処理後にコバルトシリサイド層のリーク電流がどのように異なるかを調べた特性図（その１）である。

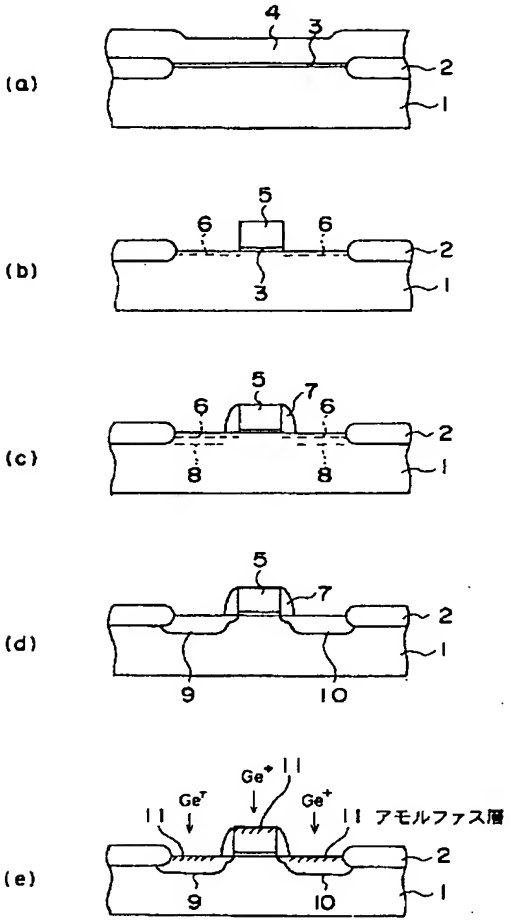
【図１９】従来方法と本発明の一実施形態に比較において、コバルト膜の膜厚の相違によって２回目熱処理後にコバルトシリサイド層のリーク電流がどのように異なるかを調べた特性図（その２）である。

【図２０】従来方法のコバルトシリサイド層の形成工程を示す断面図である。

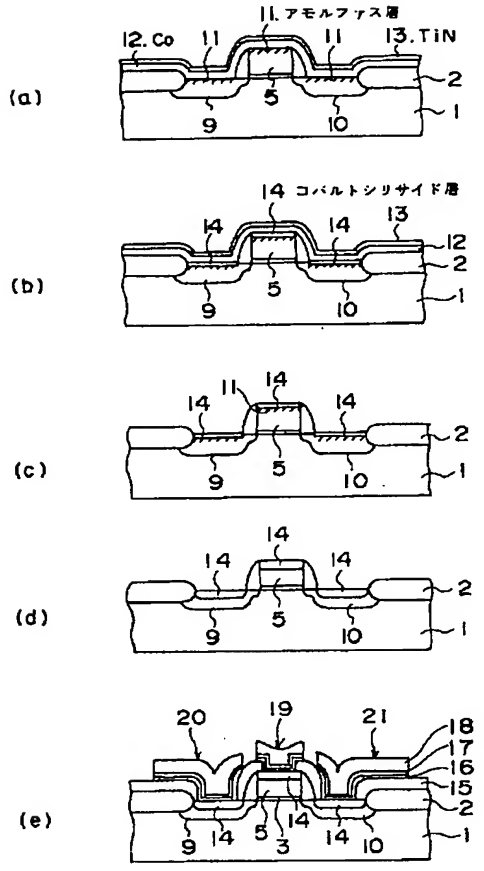
【符号の説明】

１　シリコン基板
２　ＬＯＣＯＳ酸化膜
３　ゲート酸化膜
４　ポリシリコンン膜
５　ゲート電極
６　不純物注入層
７　サイドウォール
８　不純物注入層
９　ソース層
１０　ドレイン層
１１　アモルファス層（非晶質層）
１２　コバルト膜
１３　窒化チタン膜
１４　コバルトシリサイド層

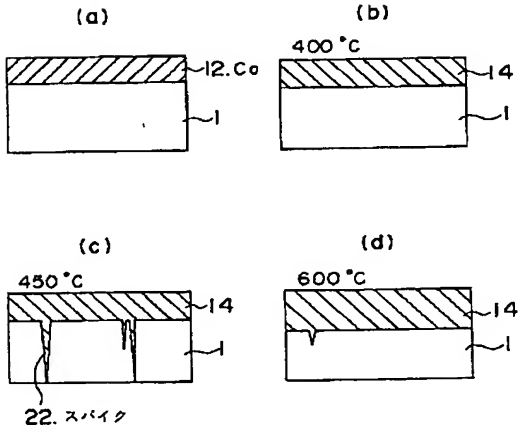
【図1】



【図2】



【図3】



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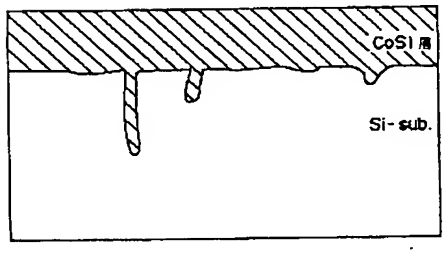
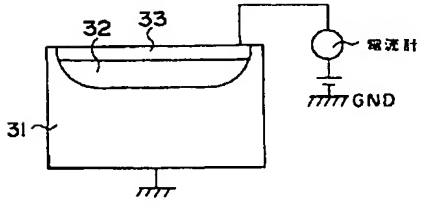


(1 st. F.A. 450 °C. 30min. ウオッシュアウト後)

【図9】



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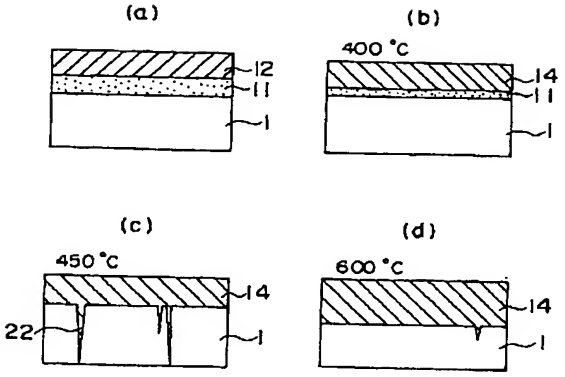
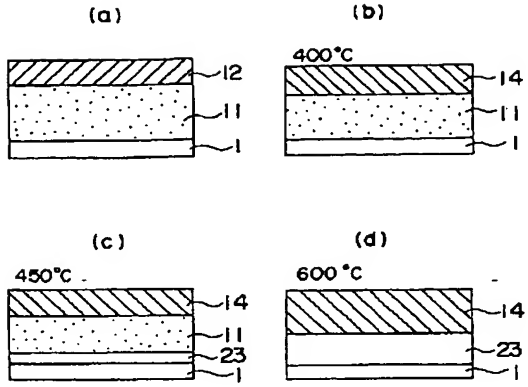


【図6】



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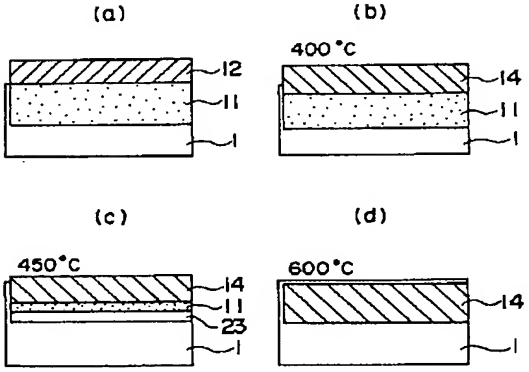
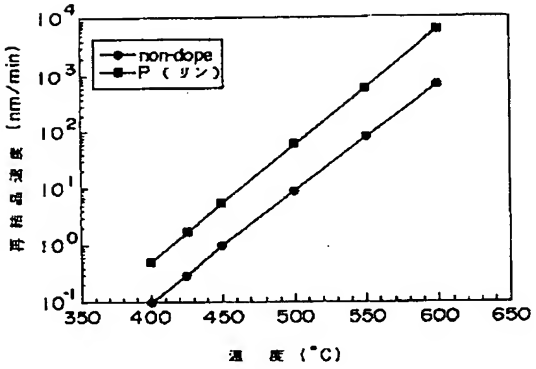


【図8】



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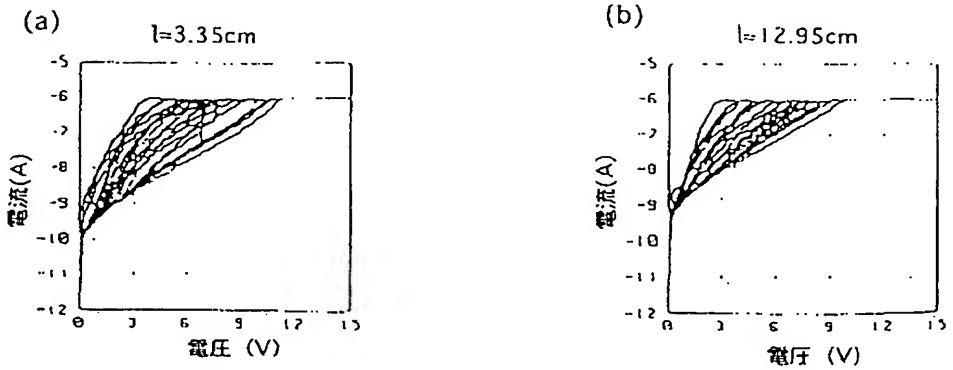
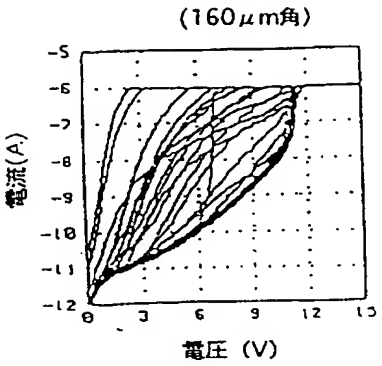
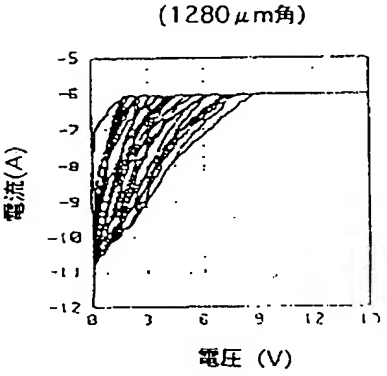


【図１０】

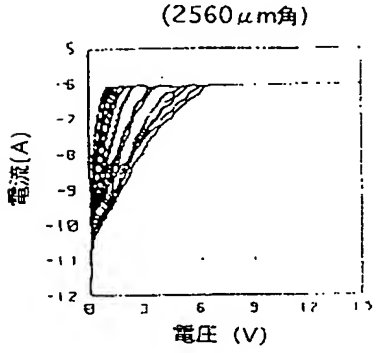
(a)



(b)

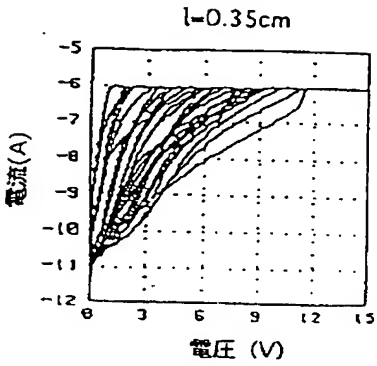


(c)

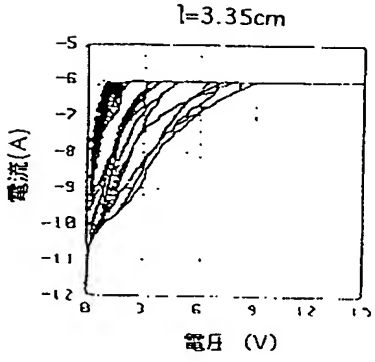


【図１１】

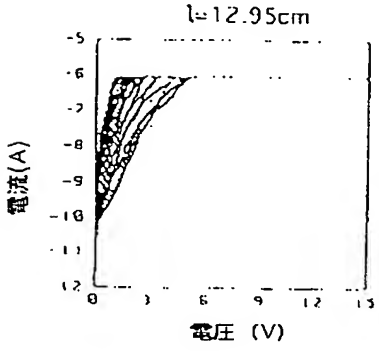
(a)



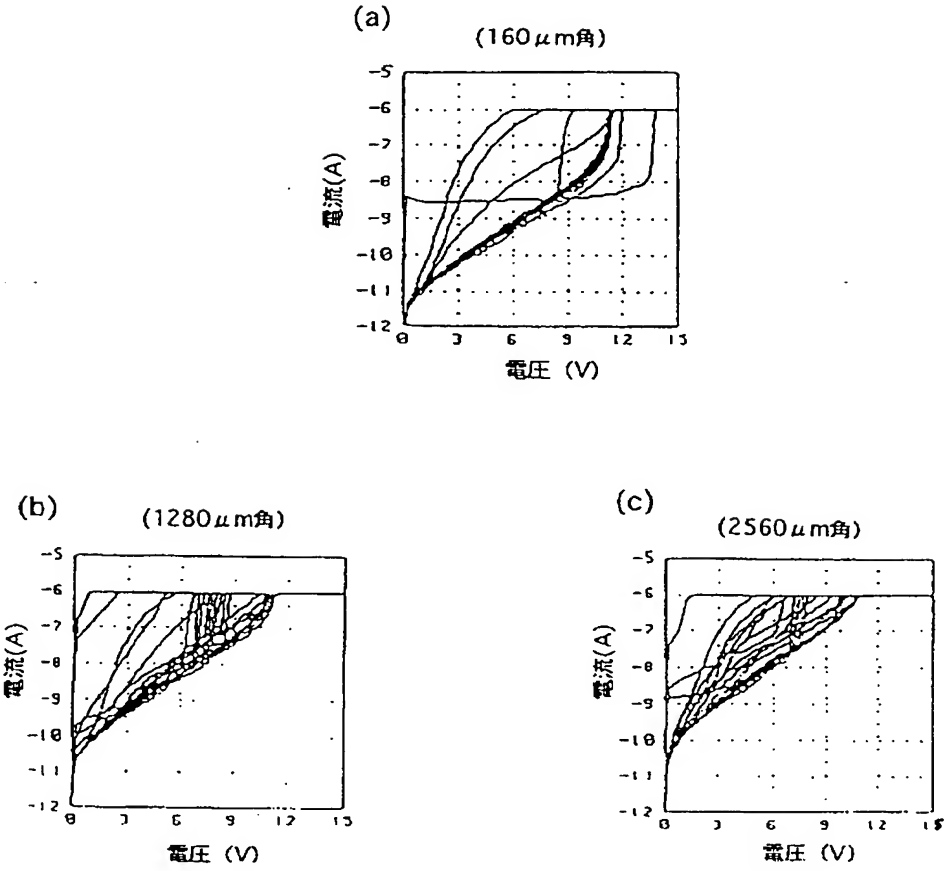
(b)



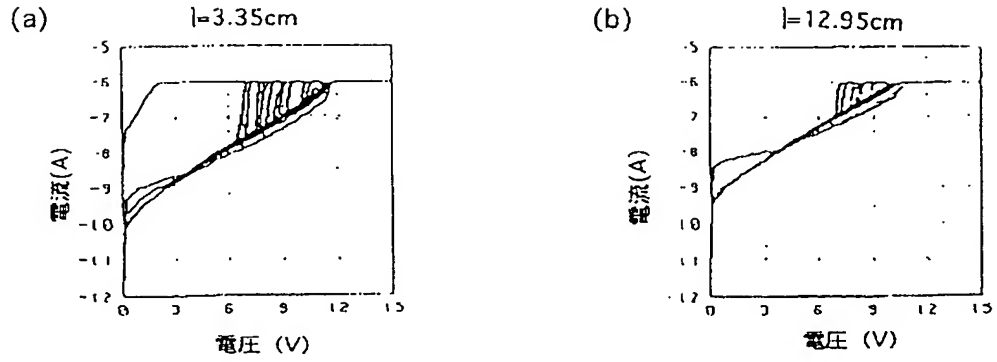
(c)



【図１２】

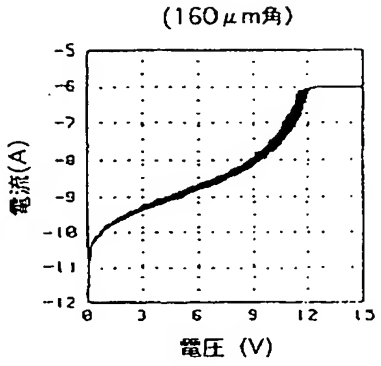

(a)
(160μm角)
電流(A)
電圧 (V)
(b)
(1280μm角)
電流(A)
電圧 (V)
(c)
(2560μm角)
電流(A)
電圧 (V)

【図１７】

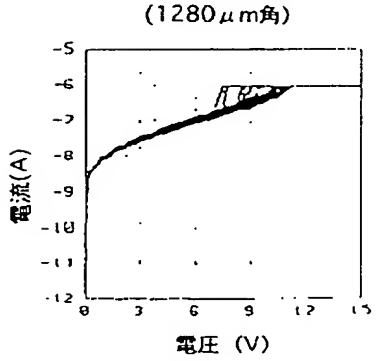

(a)
l=3.35cm
電流(A)
電圧 (V)
(b)
l=12.95cm
電流(A)
電圧 (V)

【図１４】

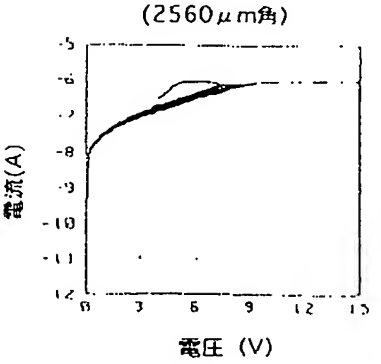
(a)



(b)

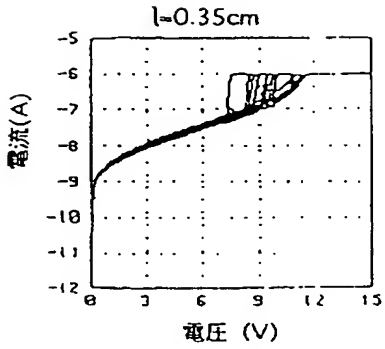


(c)

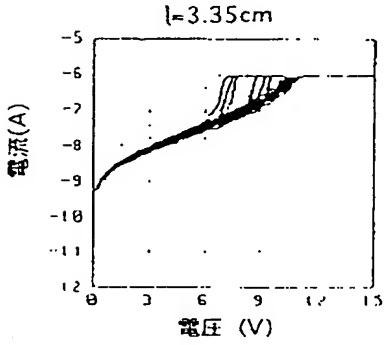


【図１５】

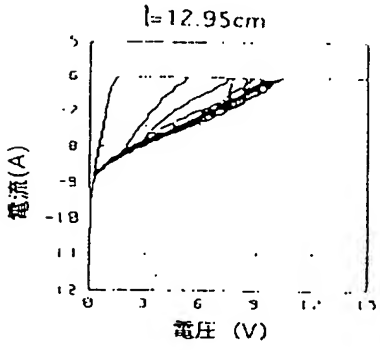
(a)



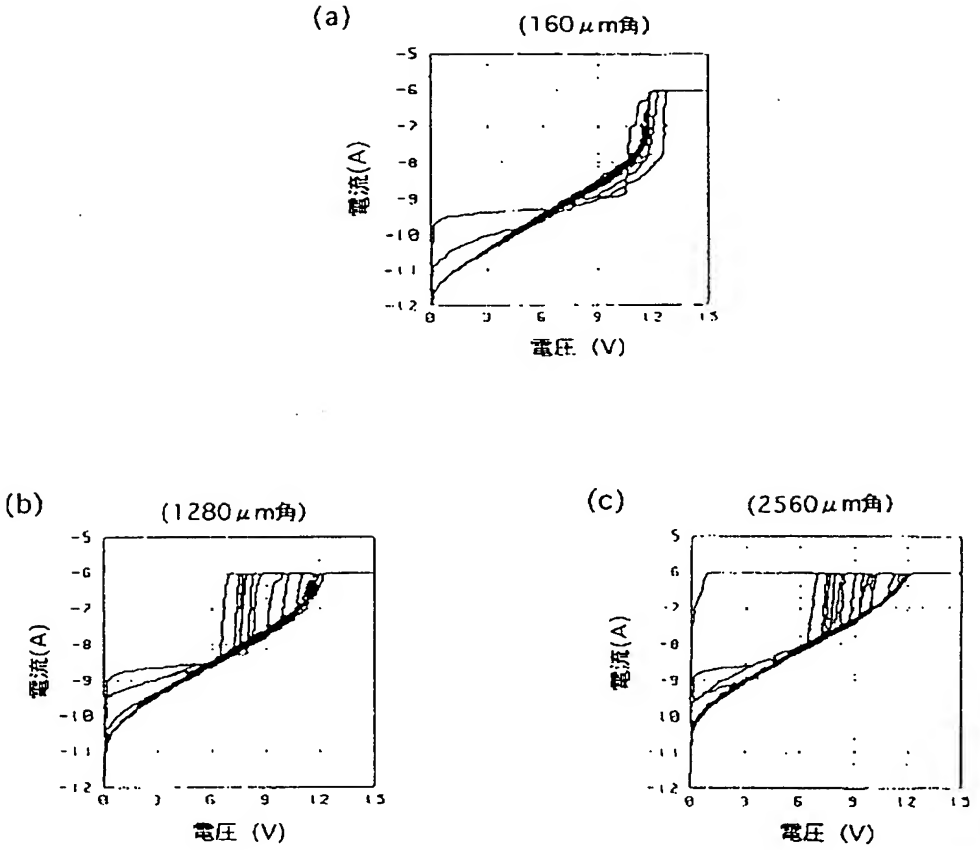
(b)



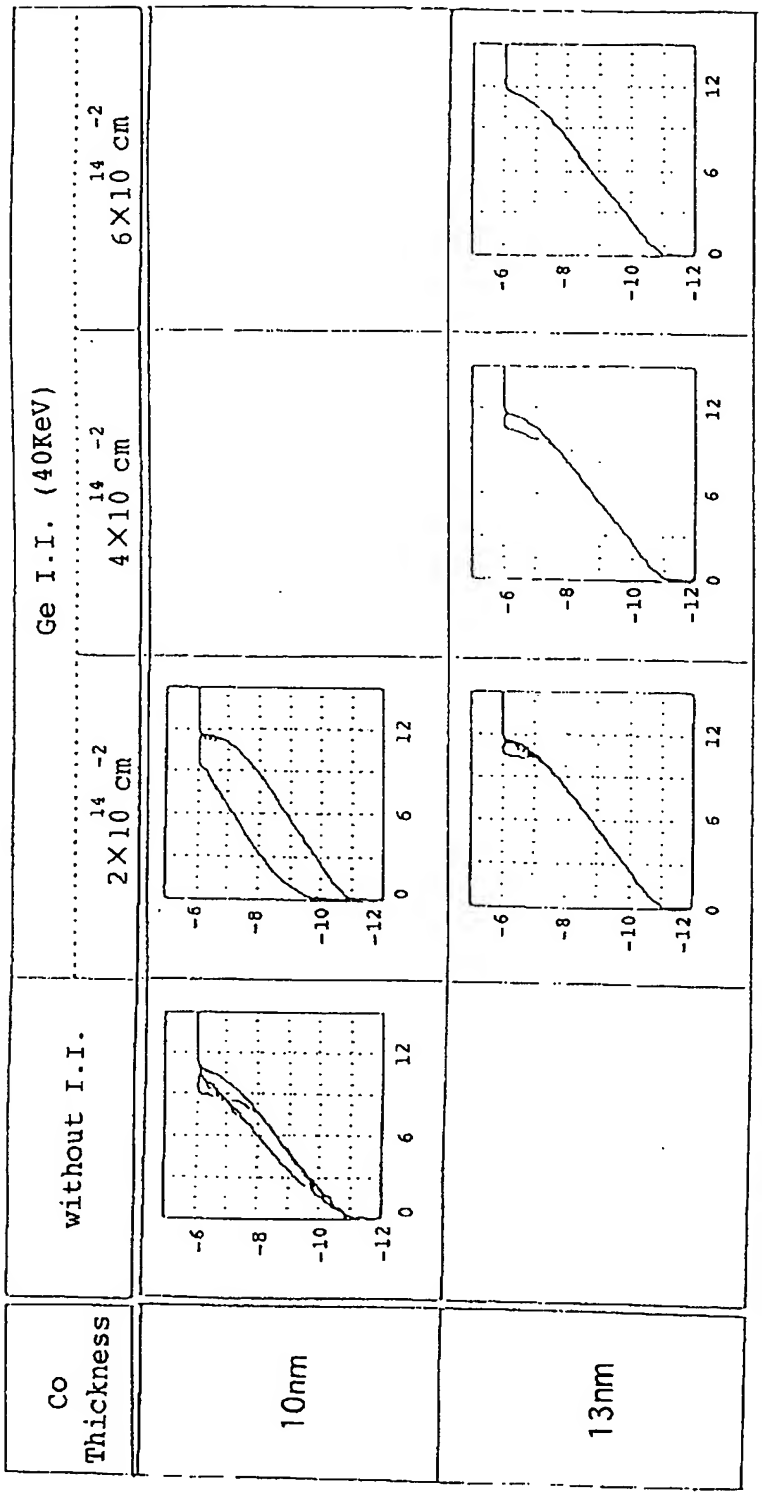
(c)



【図１６】

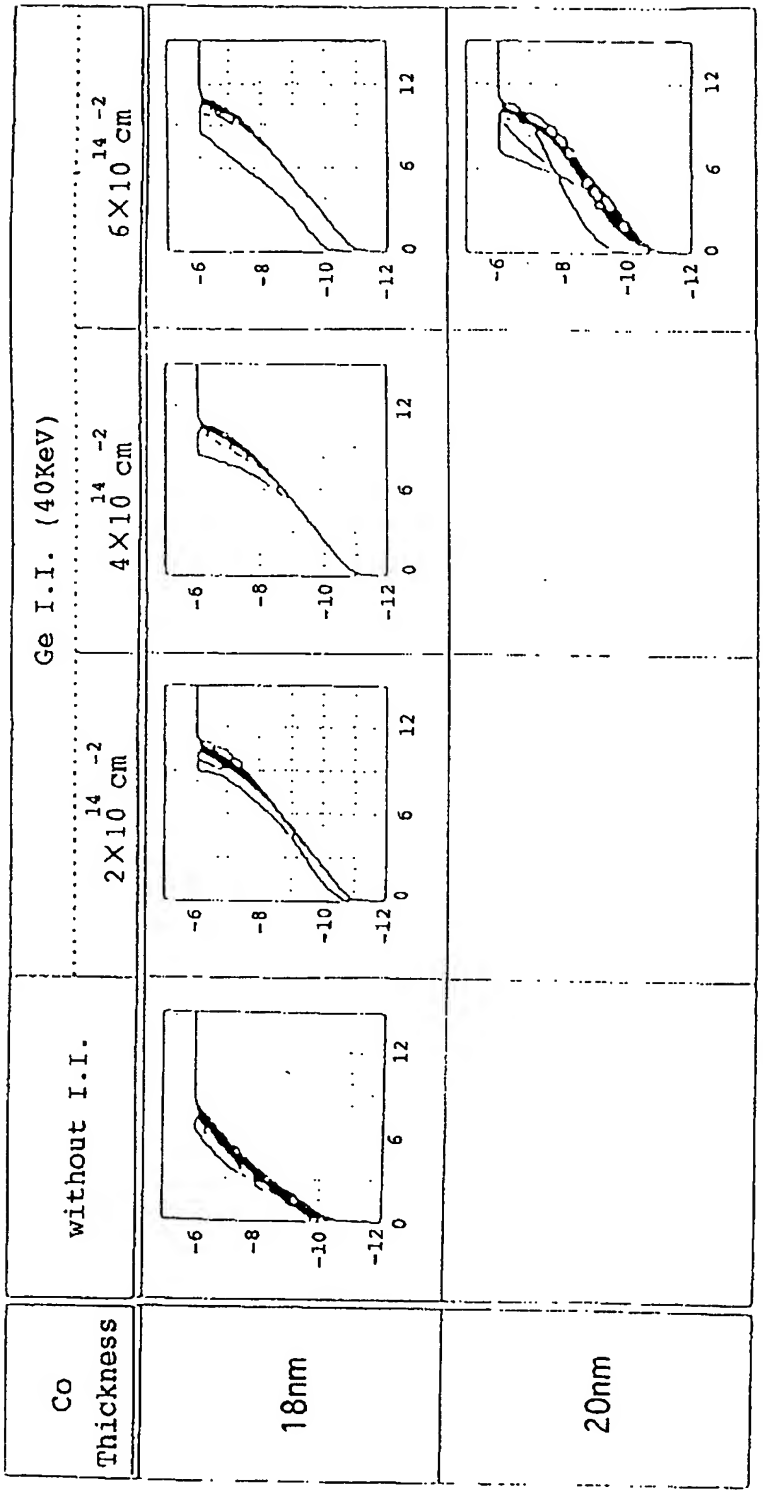


【図18】



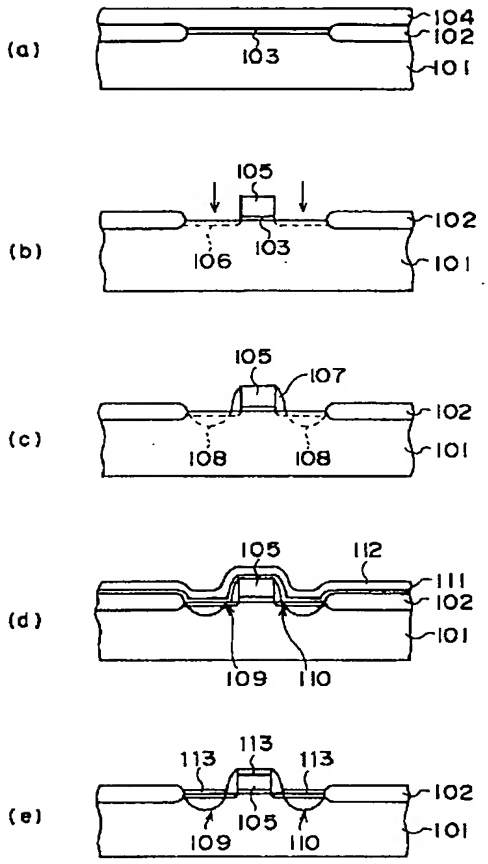
各横軸は電圧（V）を示す
各縦軸は電流（A）を示す

【図19】



各横軸は電圧（V）を示す
各縦軸は電流（A）を示す

【図20】



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